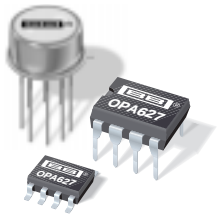
BURR - BROWN®



OPA627
OPA637

Precision High-Speed *Difet*® OPERATIONAL AMPLIFIERS

FEATURES

- VERY LOW NOISE: 4.5nV/√Hz at 10kHz
- FAST SETTLING TIME:
  OPA627—550ns to 0.01%
  OPA637—450ns to 0.01%
- LOW V_{OS}: 100μV max
- LOW DRIFT: 0.8μV/°C max
- LOW I_B: 5pA max
- OPA627: Unity-Gain Stable
- OPA637: Stable in Gain ≥ 5

APPLICATIONS

- PRECISION INSTRUMENTATION
- FAST DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- ACTIVE FILTERS

DESCRIPTION

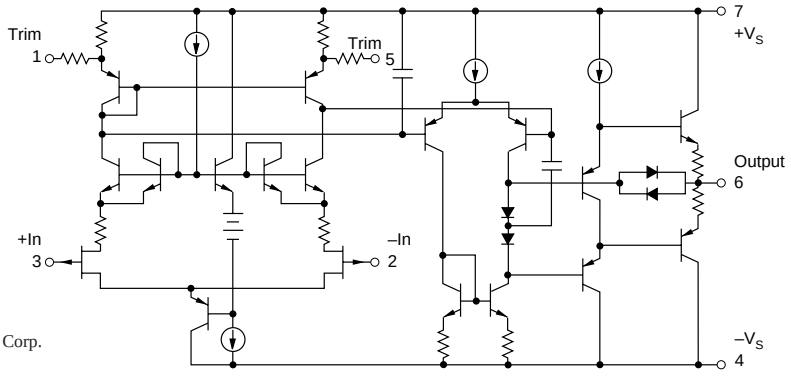
The OPA627 and OPA637 ***Difet*** operational amplifiers provide a new level of performance in a precision FET op amp. When compared to the popular OPA111 op amp, the OPA627/637 has lower noise, lower offset voltage, and much higher speed. It is useful in a broad range of precision and high speed analog circuitry.

The OPA627/637 is fabricated on a high-speed, dielectrically-isolated complementary NPN/PNP process. It operates over a wide range of power supply voltage—±4.5V to ±18V. Laser-trimmed ***Difet*** input circuitry provides high accuracy and low-noise performance comparable with the best bipolar-input op amps.

High frequency complementary transistors allow increased circuit bandwidth, attaining dynamic performance not possible with previous precision FET op amps. The OPA627 is unity-gain stable. The OPA637 is stable in gains equal to or greater than five.

Difet fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry.

The OPA627/637 is available in plastic DIP, SOIC and metal TO-99 packages. Industrial and military temperature range models are available.



Difet®, Burr-Brown Corp.

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-998H
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SBOS165

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

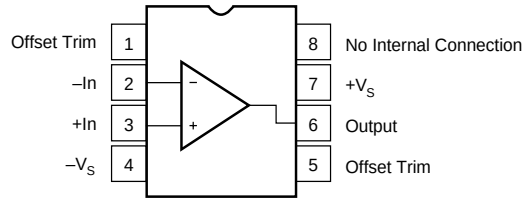
PARAMETER	CONDITIONS	OPA627BM, BP, SM OPA637BM, BP, SM MIN	TYP	MAX	OPA627AM, AP, AU OPA637AM, AP, AU MIN	TYP	MAX	UNITS
OFFSET VOLTAGE [1]								
Input Offset Voltage			40	100		130	250	µV
AP, BP, AU Grades			100	250		280	500	µV
Average Drift			0.4	0.8		1.2	2	µV/°C
AP, BP, AU Grades			0.8	2		2.5		µV/°C
Power Supply Rejection	V_S = ±4.5 to ±18V	106	120		100	116		dB
INPUT BIAS CURRENT [2]								
Input Bias Current	V_{CM} = 0V		1	5		2	10	pA
Over Specified Temperature	V_{CM} = 0V			1			2	nA
SM Grade	V_{CM} = 0V			50				nA
Over Common-Mode Voltage	V_{CM} = ±10V		1			2		pA
Input Offset Current	V_{CM} = 0V		0.5	5		1	10	pA
Over Specified Temperature	V_{CM} = 0V			1			2	nA
SM Grade				50				nA
NOISE								
Input Voltage Noise								
Noise Density: f = 10Hz			15	40		20		nV/√Hz
f = 100Hz			8	20		10		nV/√Hz
f = 1kHz			5.2	8		5.6		nV/√Hz
f = 10kHz			4.5	6		4.8		nV/√Hz
Voltage Noise, BW = 0.1Hz to 10Hz			0.6	1.6		0.8		µVp-p
Input Bias Current Noise								
Noise Density, f = 100Hz			1.6	2.5		2.5		fA/√Hz
Current Noise, BW = 0.1Hz to 10Hz			30	60		48		fAp-p
INPUT IMPEDANCE								
Differential			10^{13} || 8			*		Ω || pF
Common-Mode			10^{13} || 7			*		Ω || pF
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±11	±11.5		*	*		V
Over Specified Temperature		±10.5	±11		*	*		V
Common-Mode Rejection	V_{CM} = ±10.5V	106	116		100	110		dB
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±10V, R_L = 1kΩ	112	120		106	116		dB
Over Specified Temperature	V_O = ±10V, R_L = 1kΩ	106	117		100	110		dB
SM Grade	V_O = ±10V, R_L = 1kΩ	100	114					dB
FREQUENCY RESPONSE								
Slew Rate: OPA627	G = –1, 10V Step	40	55		*	*		V/µs
OPA637	G = –4, 10V Step	100	135		*	*		V/µs
Settling Time: OPA627 0.01%	G = –1, 10V Step		550			*		ns
0.1%	G = –1, 10V Step		450			*		ns
OPA637 0.01%	G = –4, 10V Step		450			*		ns
0.1%	G = –4, 10V Step		300			*		ns
Gain-Bandwidth Product: OPA627	G = 1		16			*		MHz
OPA637	G = 10		80			*		MHz
Total Harmonic Distortion + Noise	G = +1, f = 1kHz		0.00003			*		%
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±4.5		±18	*		*	V
Current			±7	±7.5		*	*	mA
OUTPUT								
Voltage Output	R_L = 1kΩ	±11.5	±12.3		*	*		
Over Specified Temperature		±11	±11.5		*	*		V
Current Output	V_O = ±10V		±45			*		mA
Short-Circuit Current		±35	+70/–55	±100	*	*	*	mA
Output Impedance, Open-Loop	1MHz		55			*		Ω
TEMPERATURE RANGE								
Specification: AP, BP, AM, BM, AU		–25		+85	*		*	°C
SM		–55		+125				°C
Storage: AM, BM, SM		–60		+150	*		*	°C
AP, BP, AU		–40		+125	*		*	°C
θ_{J-A}: AM, BM, SM			200			*		°C/W
AP, BP			100			*		°C/W
AU			160					°C/W

* Specifications same as "B" grade.

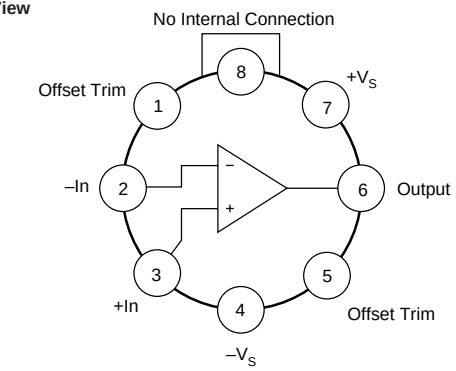
NOTES: (1) Offset voltage measured fully warmed-up. (2) High-speed test at T_J = +25°C. See Typical Performance Curves for warmed-up performance.

PIN CONFIGURATIONS

Top View **DIP/SOIC**



Top View **TO-99**



Case connected to $-V_S$.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	±18V
Input Voltage Range	$+V_S$ + 2V to $-V_S$ – 2V
Differential Input Range	Total V_S + 4V
Power Dissipation	1000mW
Operating Temperature	
M Package	–55°C to +125°C
P, U Package	–40°C to +125°C
Storage Temperature	
M Package	–65°C to +150°C
P, U Package	–40°C to +125°C
Junction Temperature	
M Package	+175°C
P, U Package	+150°C
Lead Temperature (soldering, 10s)	+300°C
SOIC (soldering, 3s)	+260°C

NOTE: (1) Stresses above these ratings may cause permanent damage.

PACKAGE/ORDERING INFORMATION

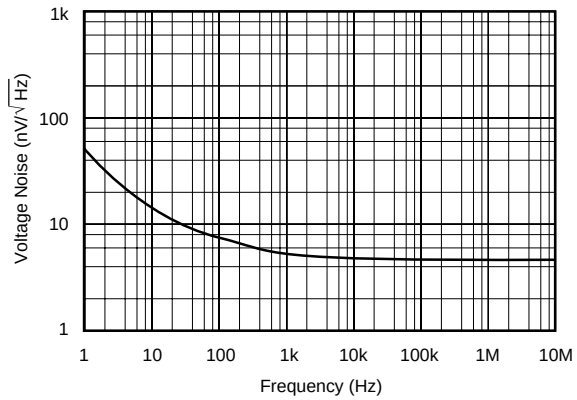
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
OPA627AP	Plastic DIP	006	–25°C to +85°C
OPA627BP	Plastic DIP	006	–25°C to +85°C
OPA627AU	SOIC	182	–25°C to +85°C
OPA627AM	TO-99 Metal	001	–25°C to +85°C
OPA627BM	TO-99 Metal	001	–25°C to +85°C
OPA627SM	TO-99 Metal	001	–55°C to +125°C
OPA637AP	Plastic DIP	006	–25°C to +85°C
OPA637BP	Plastic DIP	006	–25°C to +85°C
OPA637AU	SOIC	182	–25°C to +85°C
OPA637AM	TO-99 Metal	001	–25°C to +85°C
OPA637BM	TO-99 Metal	001	–25°C to +85°C
OPA637SM	TO-99 Metal	001	–55°C to +125°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

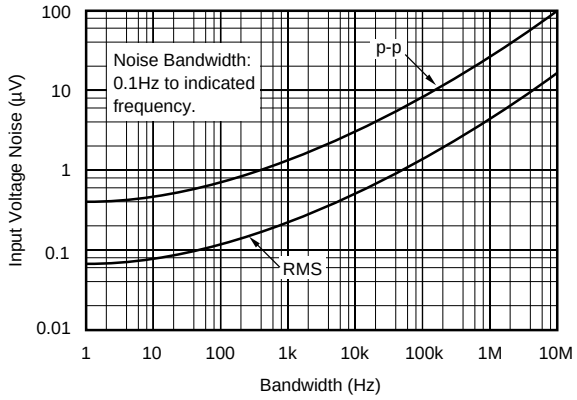
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

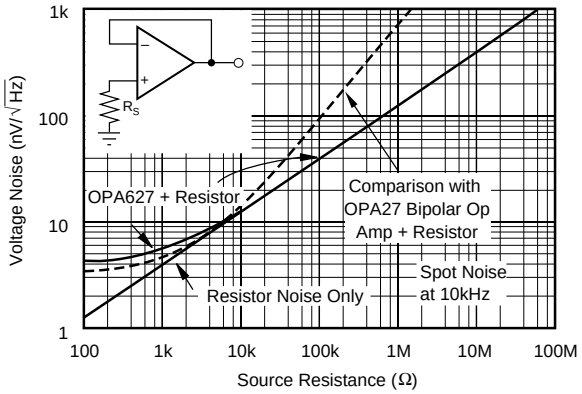
INPUT VOLTAGE NOISE SPECTRAL DENSITY



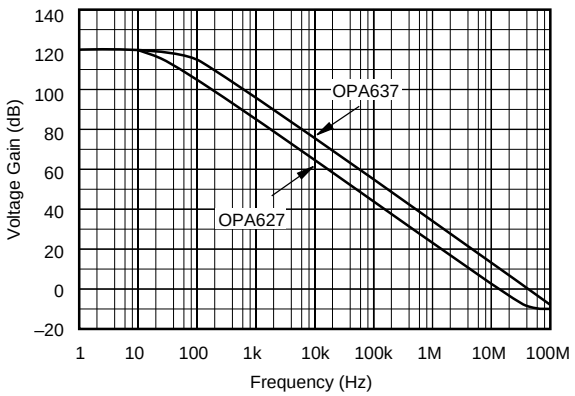
TOTAL INPUT VOLTAGE NOISE vs BANDWIDTH



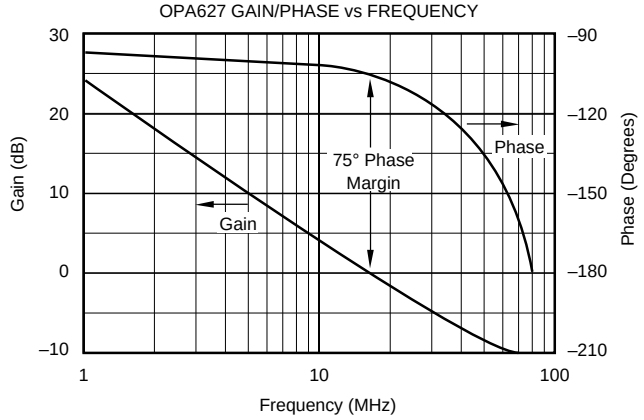
VOLTAGE NOISE vs SOURCE RESISTANCE



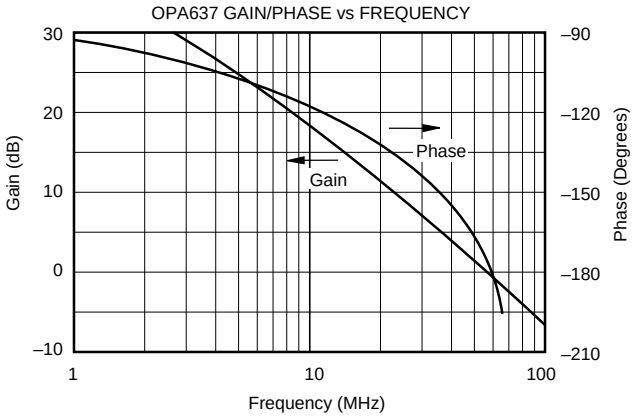
OPEN-LOOP GAIN vs FREQUENCY



OPA627 GAIN/PHASE vs FREQUENCY



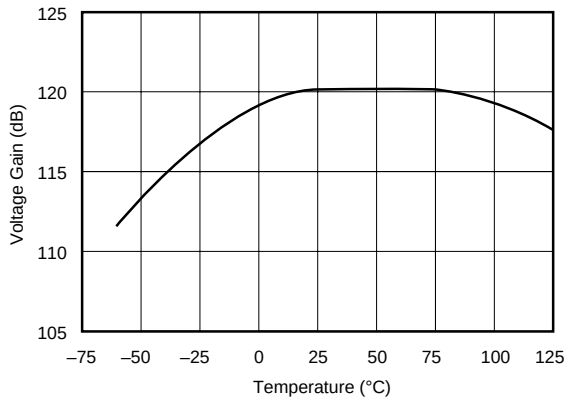
OPA637 GAIN/PHASE vs FREQUENCY



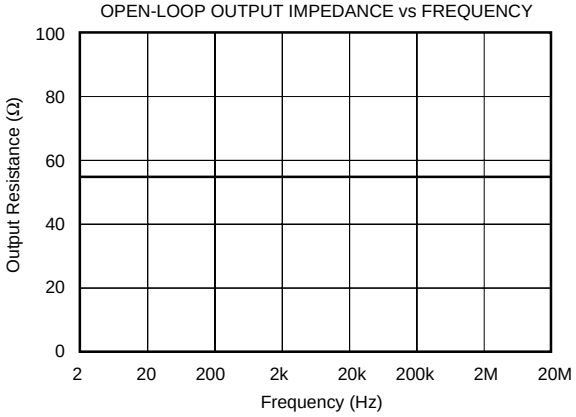
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

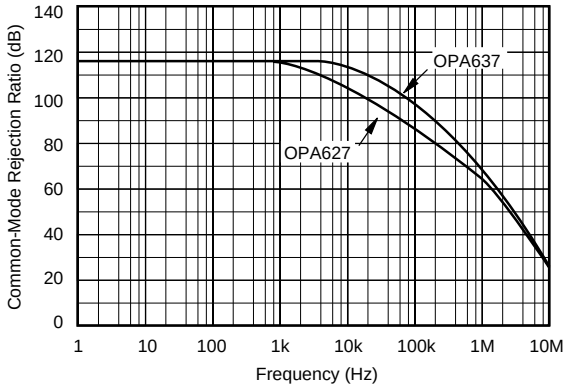
OPEN-LOOP GAIN vs TEMPERATURE



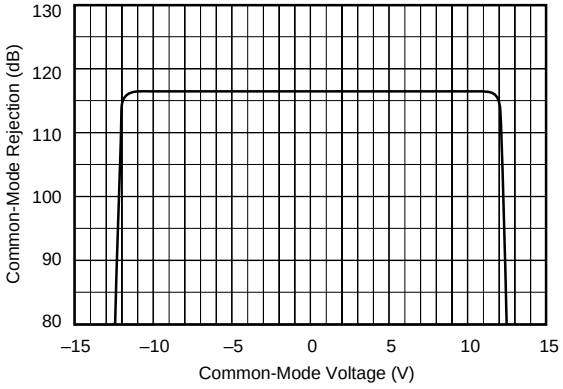
OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY



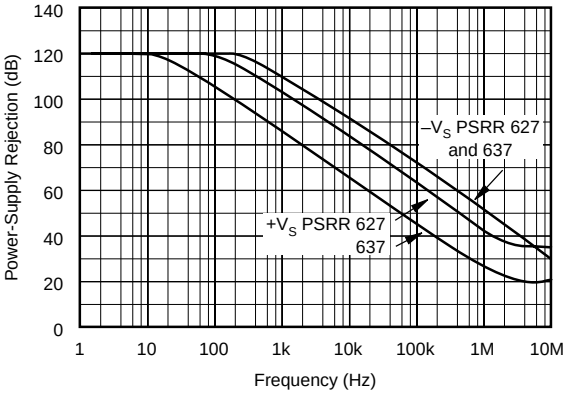
COMMON-MODE REJECTION vs FREQUENCY



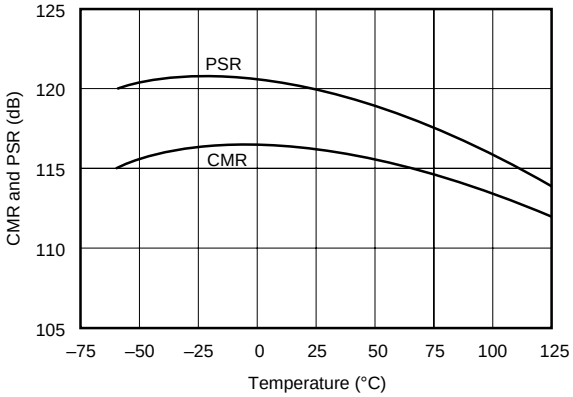
COMMON-MODE REJECTION vs
INPUT COMMON MODE VOLTAGE



POWER-SUPPLY REJECTION vs FREQUENCY



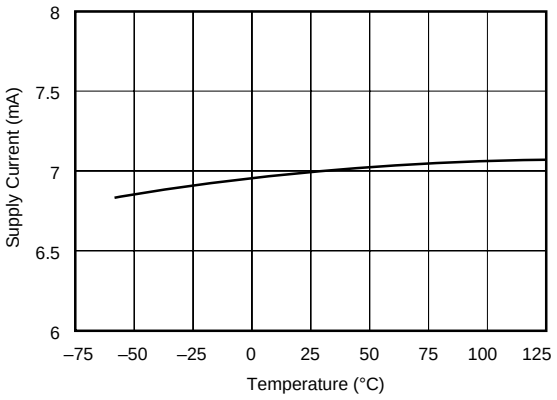
POWER-SUPPLY REJECTION AND COMMON-MODE
REJECTION vs TEMPERATURE



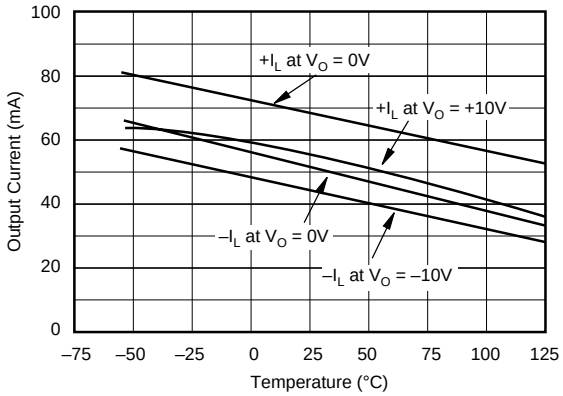
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

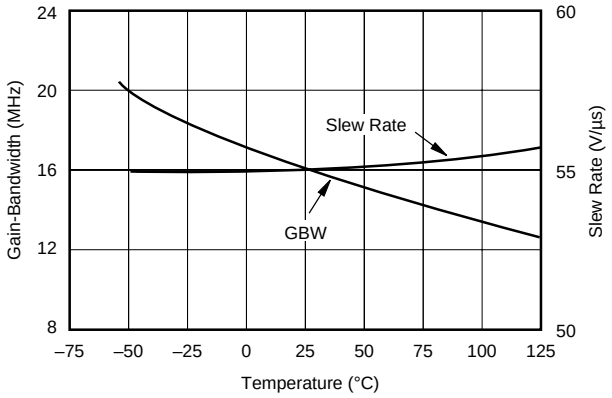
SUPPLY CURRENT vs TEMPERATURE



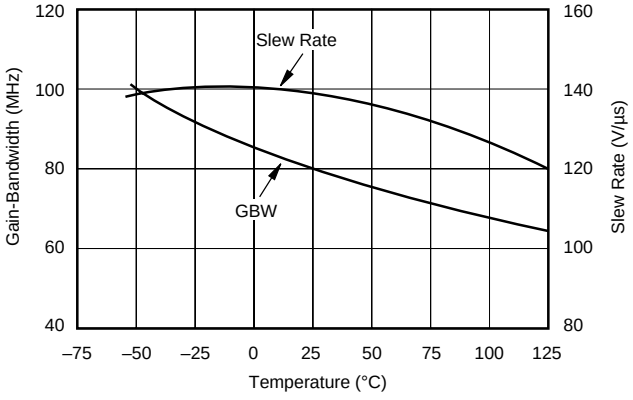
OUTPUT CURRENT LIMIT vs TEMPERATURE



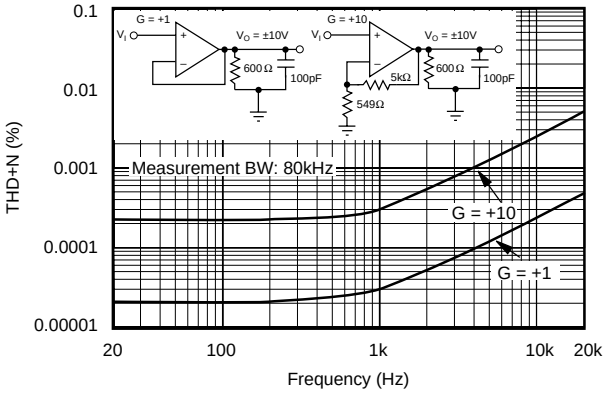
OPA627 GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



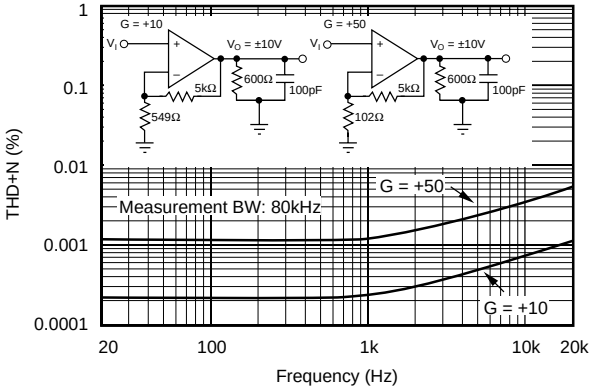
OPA637 GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



OPA627 TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



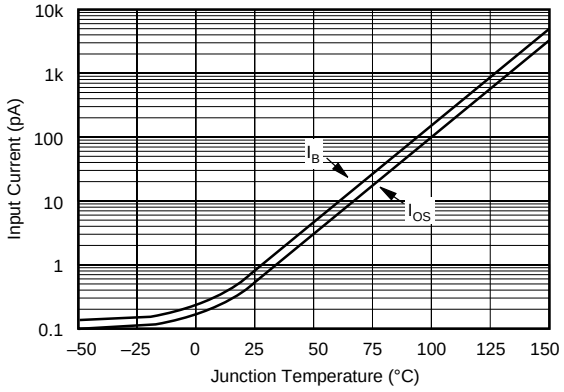
OPA637 TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



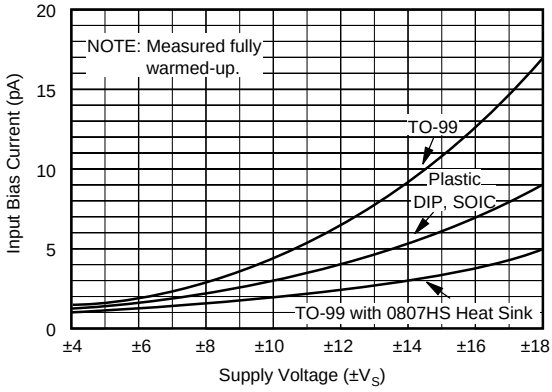
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

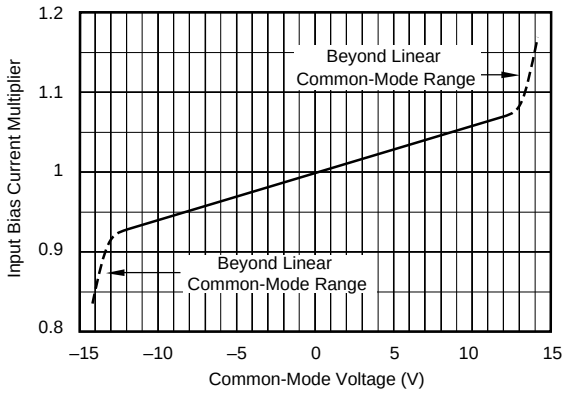
INPUT BIAS AND OFFSET CURRENT
vs JUNCTION TEMPERATURE



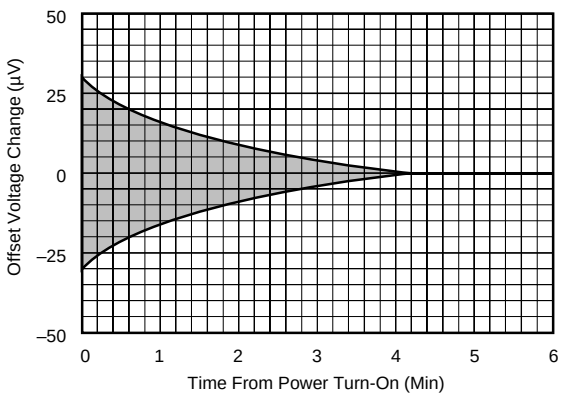
INPUT BIAS CURRENT
vs POWER SUPPLY VOLTAGE



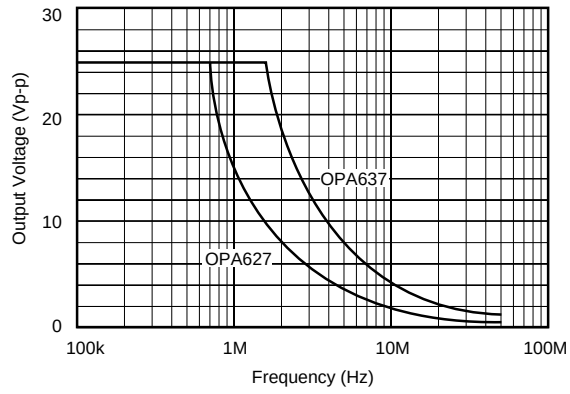
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



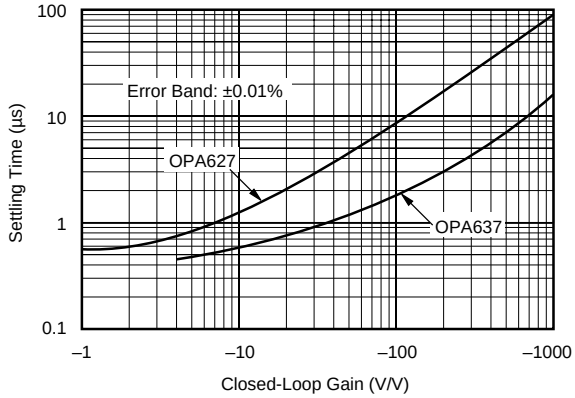
INPUT OFFSET VOLTAGE WARM-UP vs TIME



MAX OUTPUT VOLTAGE vs FREQUENCY

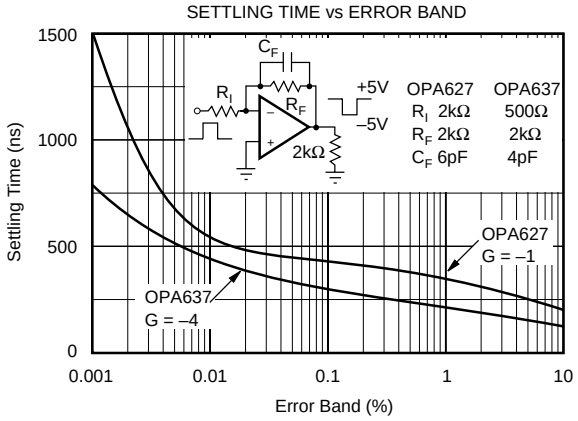


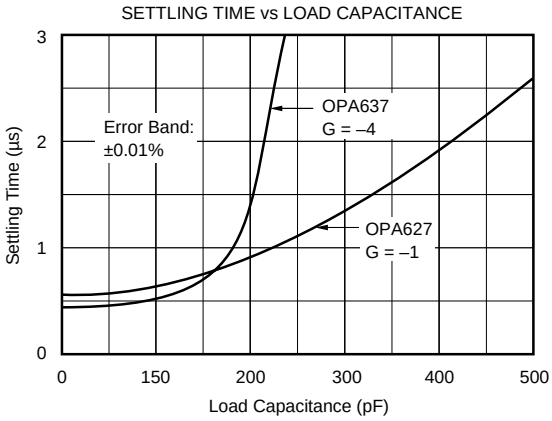
SETTLING TIME vs CLOSED-LOOP GAIN



TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.





APPLICATIONS INFORMATION

The OPA627 is unity-gain stable. The OPA637 may be used to achieve higher speed and bandwidth in circuits with noise gain greater than five. Noise gain refers to the closed-loop gain of a circuit as if the non-inverting op amp input were being driven. For example, the OPA637 may be used in a non-inverting amplifier with gain greater than five, or an inverting amplifier of gain greater than four.

When choosing between the OPA627 or OPA637, it is important to consider the high frequency noise gain of your circuit configuration. Circuits with a feedback capacitor (Figure 1) place the op amp in unity noise-gain at high frequency. These applications must use the OPA627 for proper stability. An exception is the circuit in Figure 2, where a small feedback capacitance is used to compensate for the input capacitance at the op amp's inverting input. In this case, the closed-loop noise gain remains constant with frequency, so if the closed-loop gain is equal to five or greater, the OPA637 may be used.

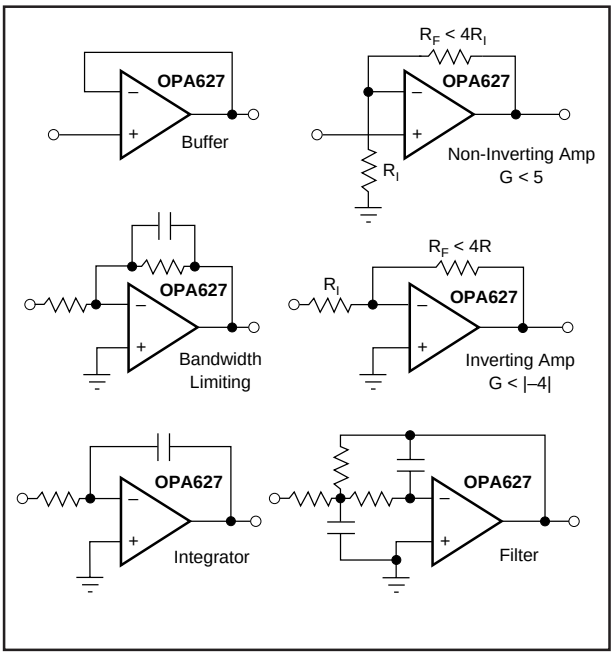


FIGURE 1. Circuits with Noise Gain Less than Five Require the OPA627 for Proper Stability.

OFFSET VOLTAGE ADJUSTMENT

The OPA627/637 is laser-trimmed for low offset voltage and drift, so many circuits will not require external adjustment. Figure 3 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system (such as in later amplification stages or in an A/D converter) because this could introduce excessive temperature drift. Generally, the offset drift will change by approximately 4µV/°C for 1mV of change in the offset voltage due to an offset adjustment (as shown on Figure 3).

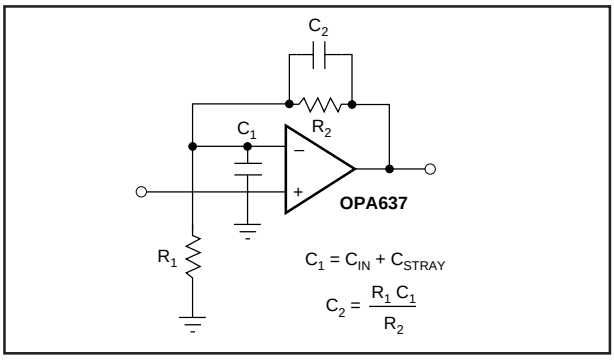


FIGURE 2. Circuits with Noise Gain Equal to or Greater than Five May Use the OPA637.

NOISE PERFORMANCE

Some bipolar op amps may provide lower voltage noise performance, but both voltage noise and bias current noise contribute to the total noise of a system. The OPA627/637 is unique in providing very low voltage noise and very low current noise. This provides optimum noise performance over a wide range of sources, including reactive source impedances. This can be seen in the performance curve showing the noise of a source resistor combined with the noise of an OPA627. Above a 2kΩ source resistance, the op amp contributes little additional noise. Below 1kΩ, op amp noise dominates over the resistor noise, but compares favorably with precision bipolar op amps.

CIRCUIT LAYOUT

As with any high speed, wide bandwidth circuit, careful layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the input pins and feedback circuitry.

The case (TO-99 metal package only) is internally connected to the negative power supply as it is with most common op amps. Pin 8 of the plastic DIP, SOIC, and TO-99 packages has no internal connection.

Power supply connections should be bypassed with good high frequency capacitors positioned close to the op amp pins. In most cases 0.1µF ceramic capacitors are adequate. The OPA627/637 is capable of high output current (in excess of 45mA). Applications with low impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors such as 1µF solid tantalum capacitors may improve dynamic performance in these applications.

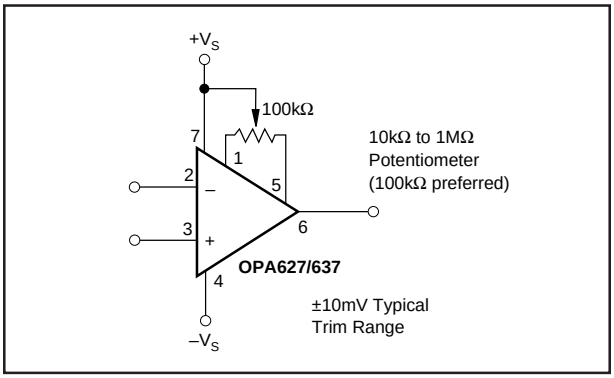


FIGURE 3. Optional Offset Voltage Trim Circuit.

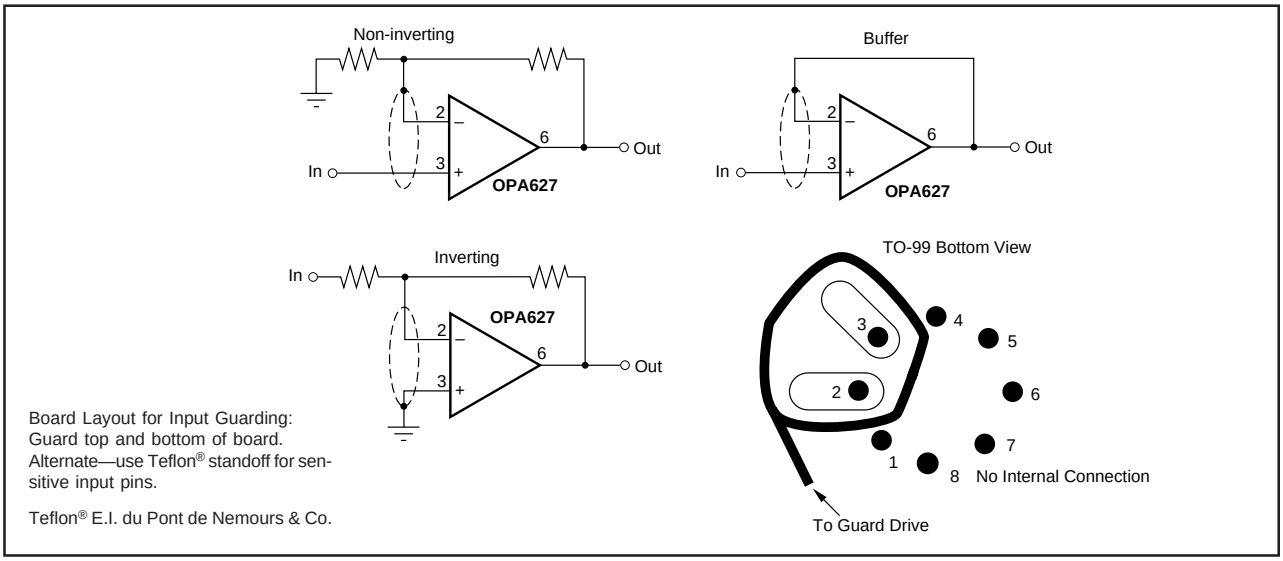


FIGURE 4. Connection of Input Guard for Lowest I_B.

INPUT BIAS CURRENT

Difet fabrication of the OPA627/637 provides very low input bias current. Since the gate current of a FET doubles approximately every 10°C, to achieve lowest input bias current, the die temperature should be kept as low as possible. The high speed and therefore higher quiescent current of the OPA627/637 can lead to higher chip temperature. A simple press-on heat sink such as the Burr-Brown model 807HS (TO-99 metal package) can reduce chip temperature by approximately 15°C, lowering the I_B to one-third its warmed-up value. The 807HS heat sink can also reduce low-frequency voltage noise caused by air currents and thermoelectric effects. See the data sheet on the 807HS for details.

Temperature rise in the plastic DIP and SOIC packages can be minimized by soldering the device to the circuit board. Wide copper traces will also help dissipate heat.

The OPA627/637 may also be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using ±5V power supplies reduces power dissipation to one-third of that at ±15V. This reduces the I_B of TO-99 metal package devices to approximately one-fourth the value at ±15V.

Leakage currents between printed circuit board traces can easily exceed the input bias current of the OPA627/637. A circuit board "guard" pattern (Figure 4) reduces leakage effects. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage current will flow harmlessly to the low-impedance node. The case (TO-99 metal package only) is internally connected to $-V_S$.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be removed with cleaning solvents and deionized water. Each rinsing operation should be followed by a 30-minute bake at 85°C.

Many FET-input op amps exhibit large changes in input bias current with changes in input voltage. Input stage cascode circuitry makes the input bias current of the OPA627/637 virtually constant with wide common-mode voltage changes. This is ideal for accurate high input-impedance buffer applications.

PHASE-REVERSAL PROTECTION

The OPA627/637 has internal phase-reversal protection. Many FET-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This is most often encountered in non-inverting circuits when the input is driven below –12V, causing the output to reverse into the positive rail. The input circuitry of the OPA627/637 does not induce phase reversal with excessive common-mode voltage, so the output limits into the appropriate rail.

OUTPUT OVERLOAD

When the inputs to the OPA627/637 are overdriven, the output voltage of the OPA627/637 smoothly limits at approximately 2.5V from the positive and negative power supplies. If driven to the negative swing limit, recovery takes approximately 500ns. When the output is driven into the positive limit, recovery takes approximately 6µs. Output recovery of the OPA627 can be improved using the output clamp circuit shown in Figure 5. Diodes at the inverting input prevent degradation of input bias current.

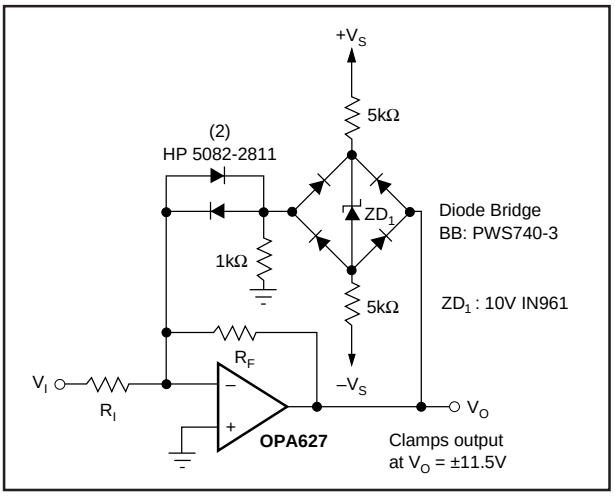


FIGURE 5. Clamp Circuit for Improved Overload Recovery.

CAPACITIVE LOADS

As with any high-speed op amp, best dynamic performance can be achieved by minimizing the capacitive load. Since a load capacitance presents a decreasing impedance at higher frequency, a load capacitance which is easily driven by a slow op amp can cause a high-speed op amp to perform poorly. See the typical curves showing settling times as a function of capacitive load. The lower bandwidth of the OPA627 makes it the better choice for driving large capacitive loads. Figure 6 shows a circuit for driving very large load capacitance. This circuit's two-pole response can also be used to sharply limit system bandwidth. This is often useful in reducing the noise of systems which do not require the full bandwidth of the OPA627.

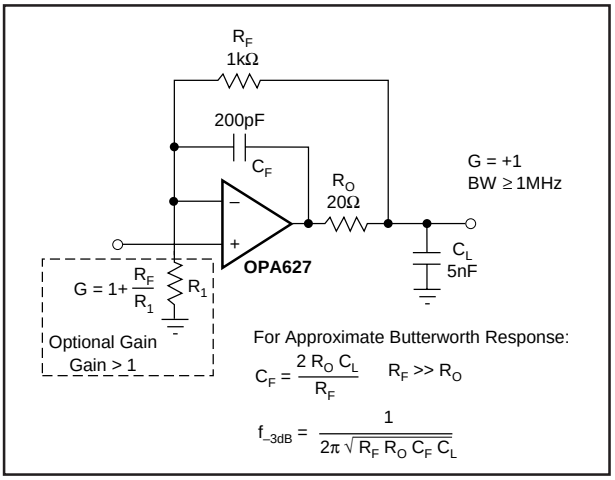


FIGURE 6. Driving Large Capacitive Loads.

INPUT PROTECTION

The inputs of the OPA627/637 are protected for voltages between $+V_S$ + 2V and $-V_S$ – 2V. If the input voltage can exceed these limits, the amplifier should be protected. The diode clamps shown in Figure 7a will prevent the input voltage from exceeding one forward diode voltage drop beyond the power supplies—well within the safe limits. If the input source can deliver current in excess of the maximum forward current of the protection diodes, use a series resistor, R_S, to limit the current. Be aware that adding resistance to the input will increase noise. The $4nV/\sqrt{Hz}$ theoretical thermal noise of a 1kΩ resistor will add to the $4.5nV/\sqrt{Hz}$ noise of the OPA627/637 (by the square-root of the sum of the squares), producing a total noise of $6nV/\sqrt{Hz}$. Resistors below 100Ω add negligible noise.

Leakage current in the protection diodes can increase the total input bias current of the circuit. The specified maximum leakage current for commonly used diodes such as the 1N4148 is approximately 25nA—more than a thousand times larger than the input bias current of the OPA627/637. Leakage current of these diodes is typically much lower and may be adequate in many applications. Light falling on the junction of the protection diodes can dramatically increase leakage current, so common glass-packaged diodes should be shielded from ambient light. Very low leakage can be achieved by using a diode-connected FET as shown. The 2N4117A is specified at 1pA and its metal case shields the junction from light.

Sometimes input protection is required on I/V converters of inverting amplifiers (Figure 7b). Although in normal operation, the voltage at the summing junction will be near zero (equal to the offset voltage of the amplifier), large input transients may cause this node to exceed 2V beyond the power supplies. In this case, the summing junction should be protected with diode clamps connected to ground. Even with the low voltage present at the summing junction, common signal diodes may have excessive leakage current. Since the reverse voltage on these diodes is clamped, a diode-connected signal transistor can be used as an inexpensive low leakage diode (Figure 7b).

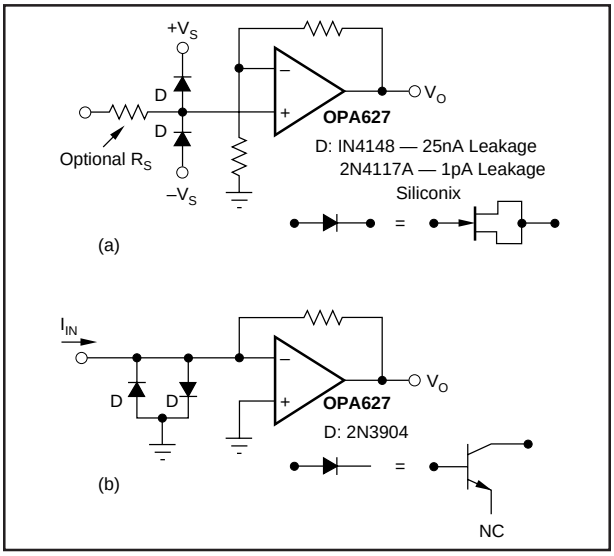


FIGURE 7. Input Protection Circuits.

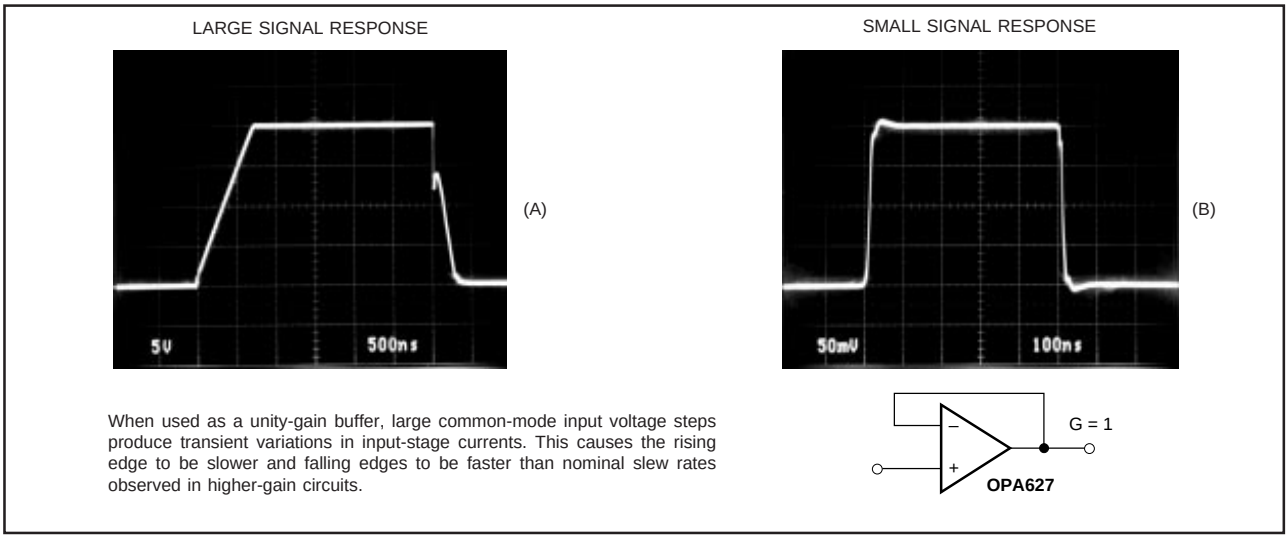


FIGURE 8. OPA627 Dynamic Performance, G = +1.

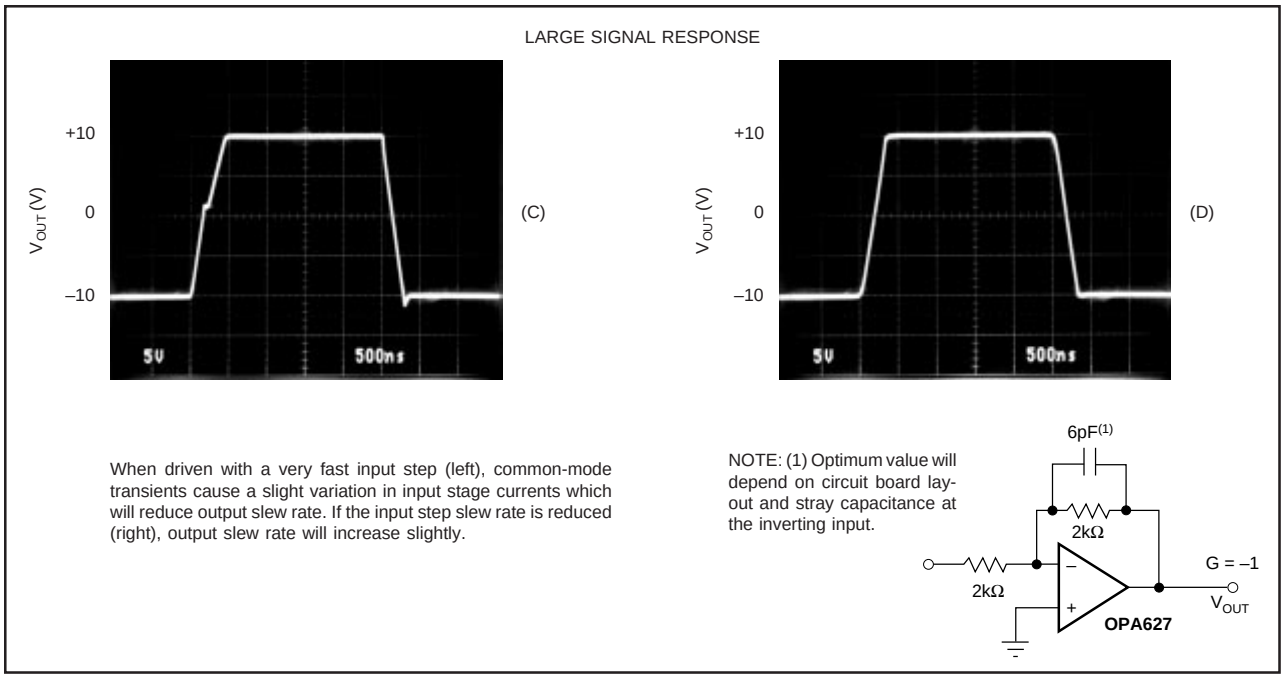


FIGURE 9. OPA627 Dynamic Performance, G = –1.

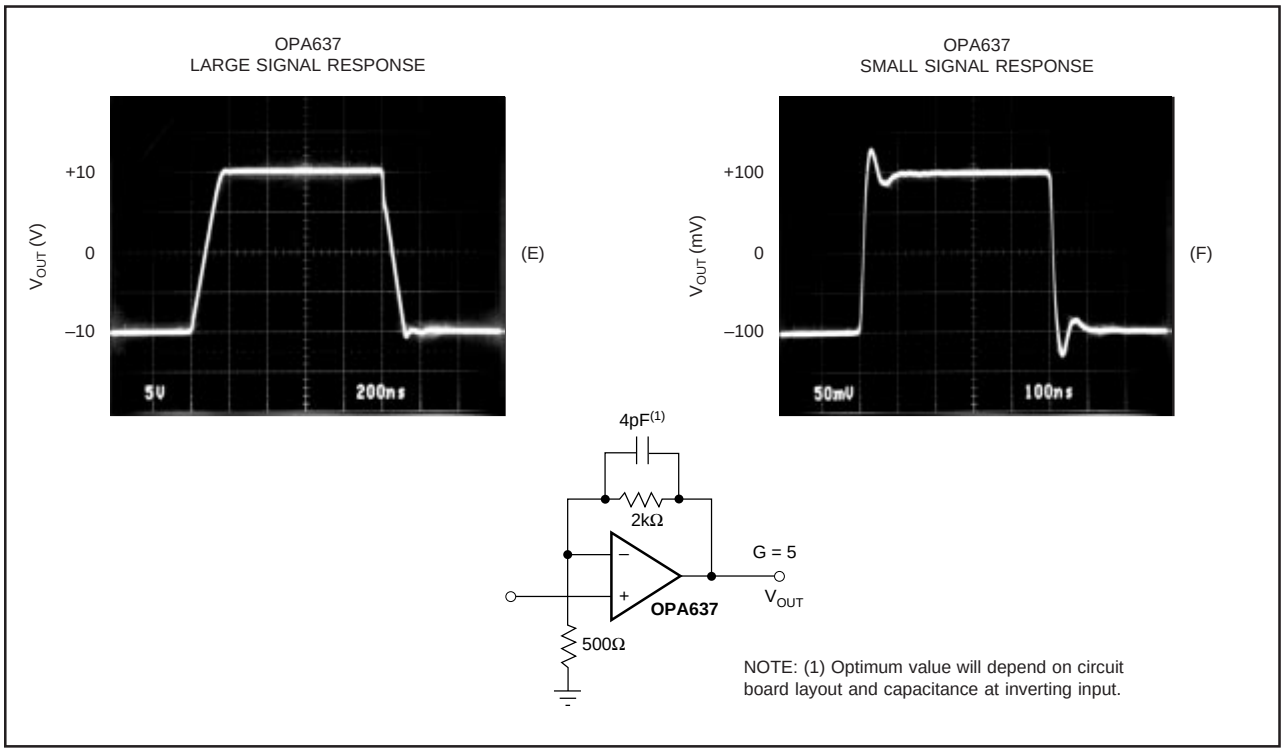
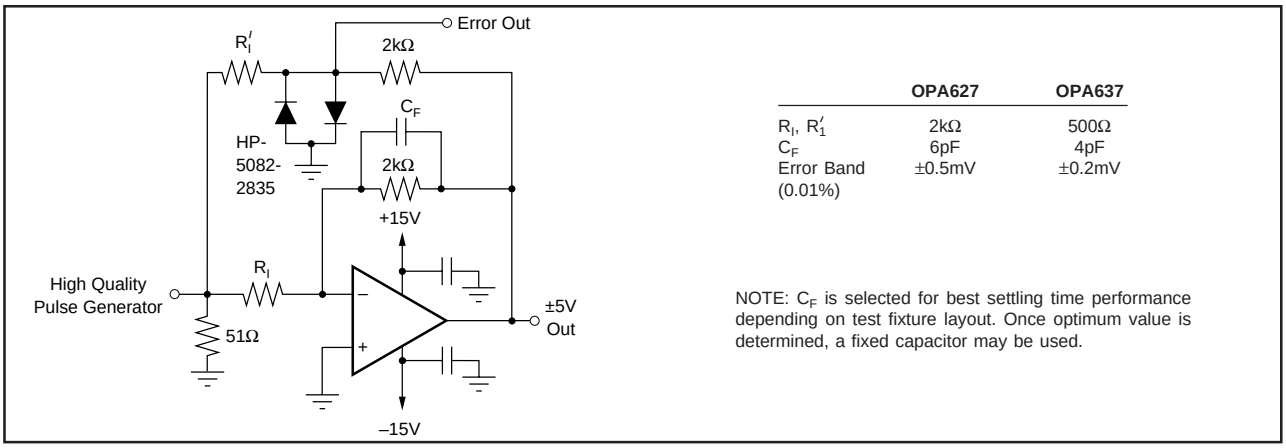


FIGURE 10. OPA637 Dynamic Response, G = 5.



	OPA627	OPA637
R_I, R_1'	2kΩ	500Ω
C_F	6pF	4pF
Error Band (0.01%)	±0.5mV	±0.2mV

NOTE: C_F is selected for best settling time performance depending on test fixture layout. Once optimum value is determined, a fixed capacitor may be used.

FIGURE 11. Settling Time and Slew Rate Test Circuit.

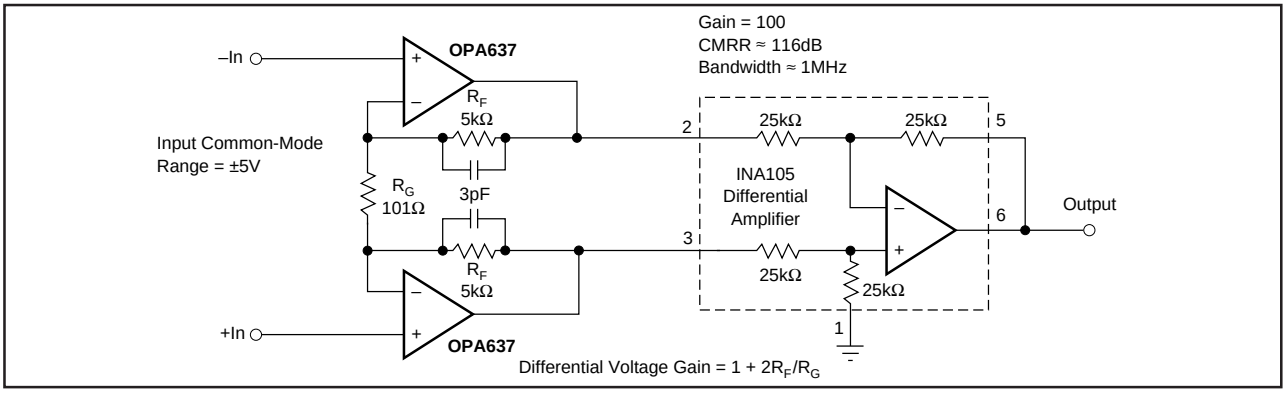


FIGURE 12. High Speed Instrumentation Amplifier, Gain = 100.

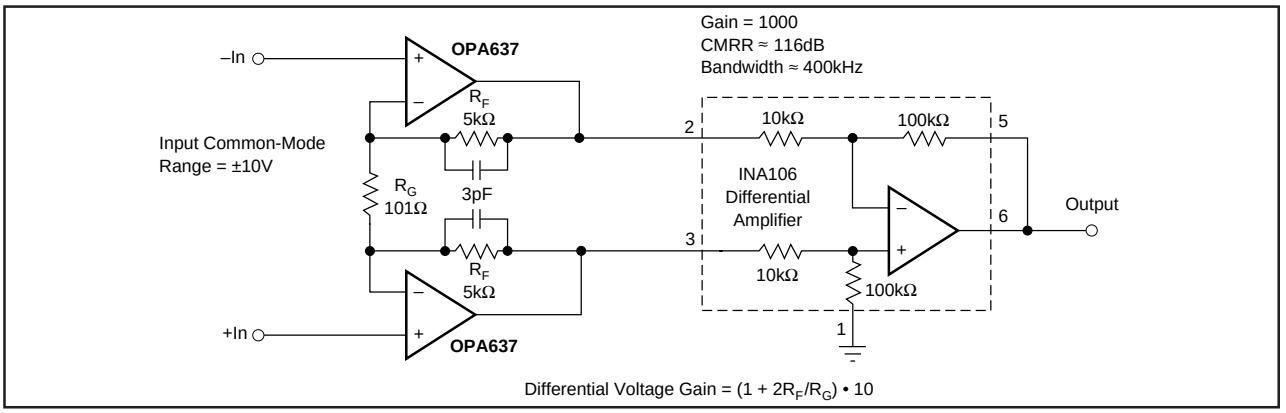
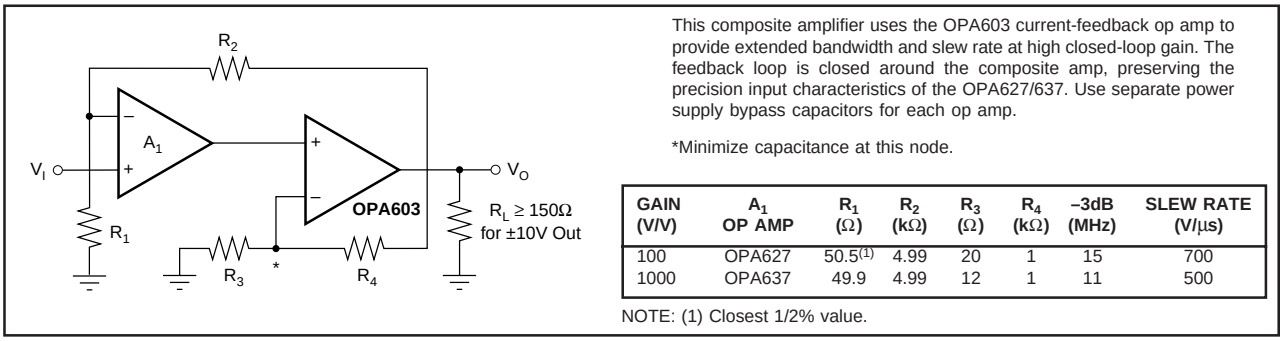


FIGURE 13. High Speed Instrumentation Amplifier, Gain = 1000.



This composite amplifier uses the OPA603 current-feedback op amp to provide extended bandwidth and slew rate at high closed-loop gain. The feedback loop is closed around the composite amp, preserving the precision input characteristics of the OPA627/637. Use separate power supply bypass capacitors for each op amp.

*Minimize capacitance at this node.

GAIN (V/V)	A_1 OP AMP	R_1 (Ω)	R_2 (kΩ)	R_3 (Ω)	R_4 (kΩ)	–3dB (MHz)	SLEW RATE (V/μs)
100	OPA627	50.5(1)	4.99	20	1	15	700
1000	OPA637	49.9	4.99	12	1	11	500

NOTE: (1) Closest 1/2% value.

FIGURE 14. Composite Amplifier for Wide Bandwidth.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA627AM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type
OPA627AP	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI
OPA627APG4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI
OPA627AU	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA627AU/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA627AU/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA627AUE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA627AUG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA627BM	NRND	TO-99	LMC	8	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type
OPA627BP	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI
OPA627BPG4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI
OPA627SM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type
OPA637AM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type
OPA637AM2	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI
OPA637AP	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI
OPA637APG4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI
OPA637AU	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA637AU/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA637AU/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA637AUE4	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
OPA637AUG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA637BM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type
OPA637BM1	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI
OPA637BP	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI
OPA637BPG4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI
OPA637SM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type

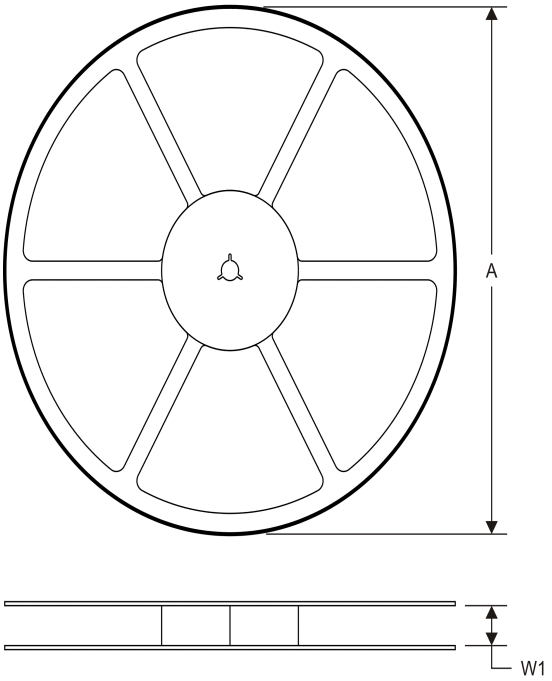
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

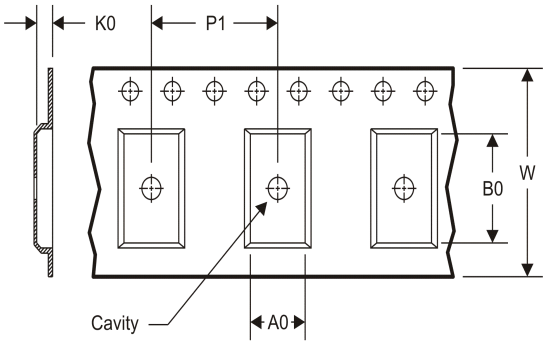
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



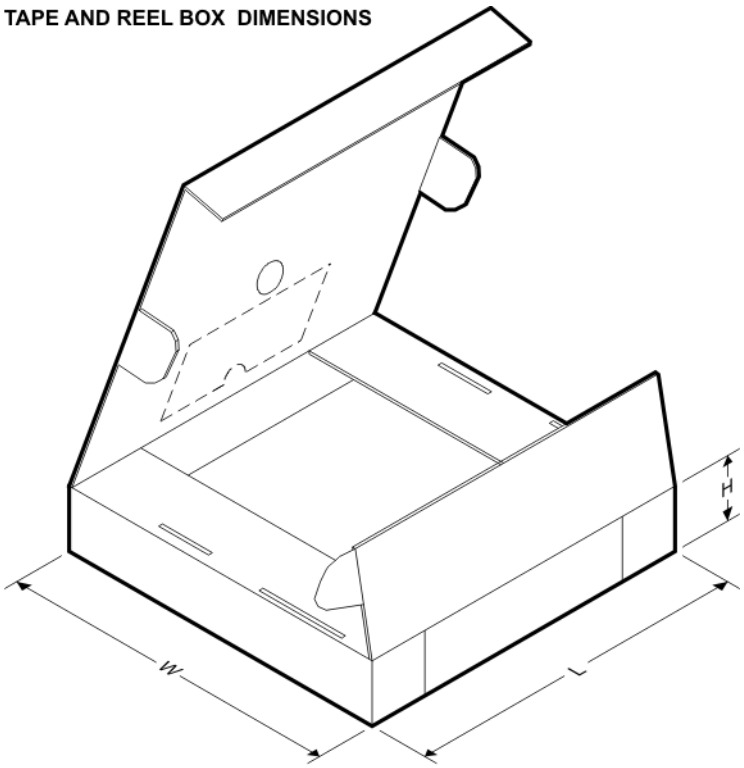
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA637AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

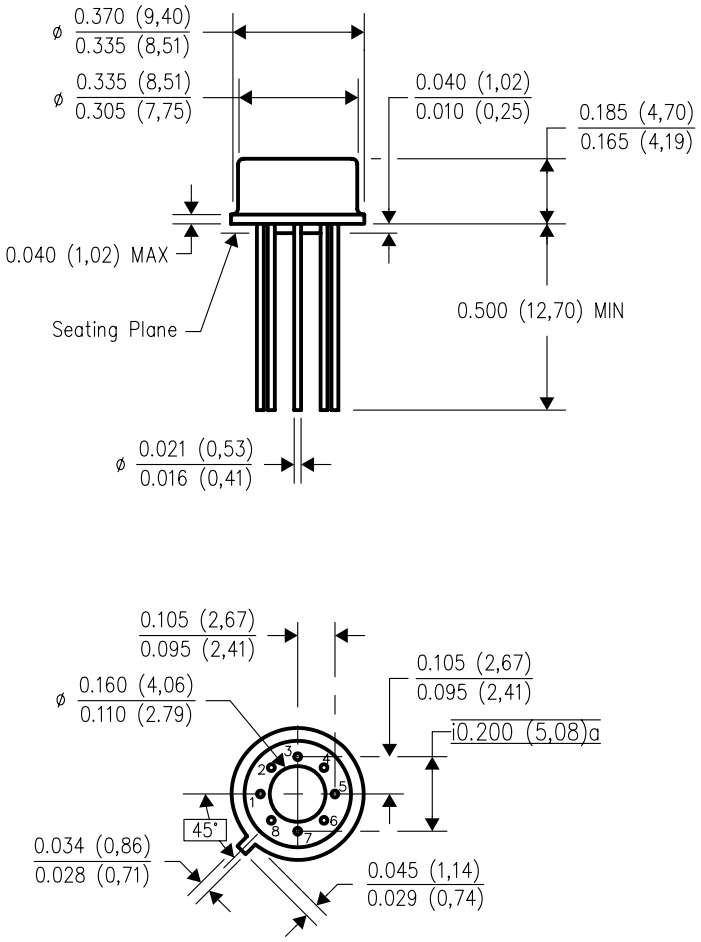
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA637AU/2K5	SOIC	D	8	2500	367.0	367.0	35.0

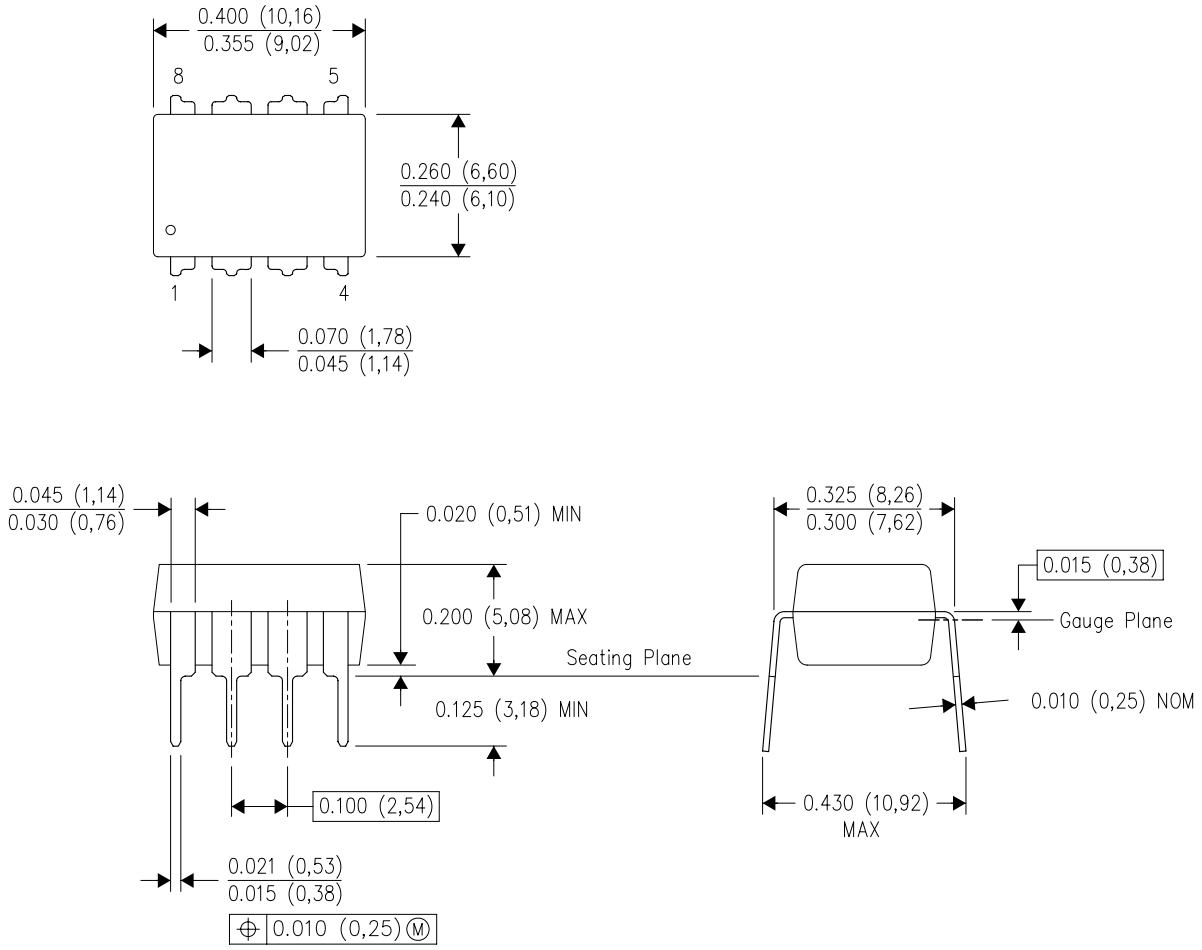
LMC (O–MBCY–W8) METAL CYLINDRICAL PACKAGE



4202483/B 09/07

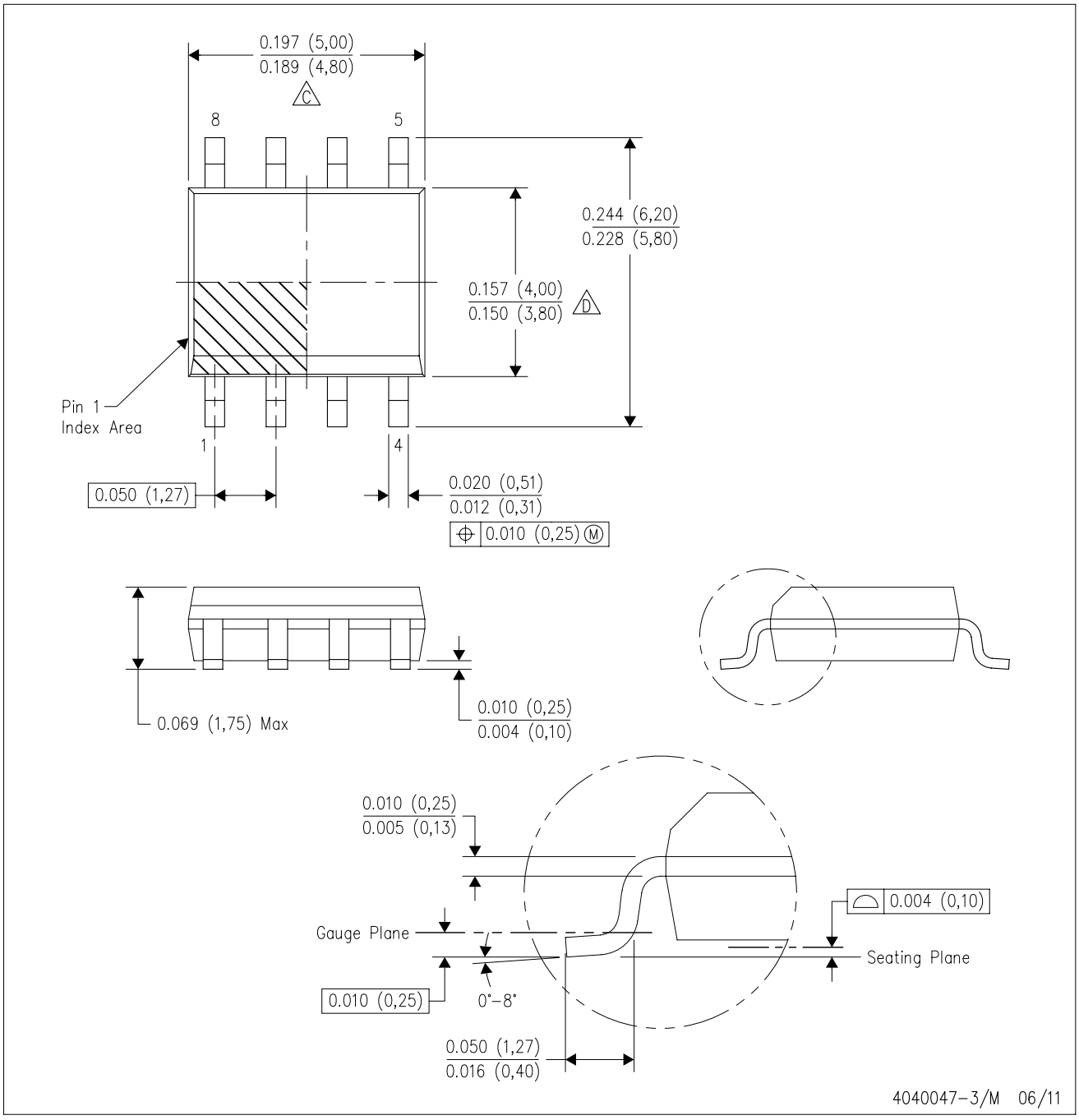
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO–002/TO–99.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



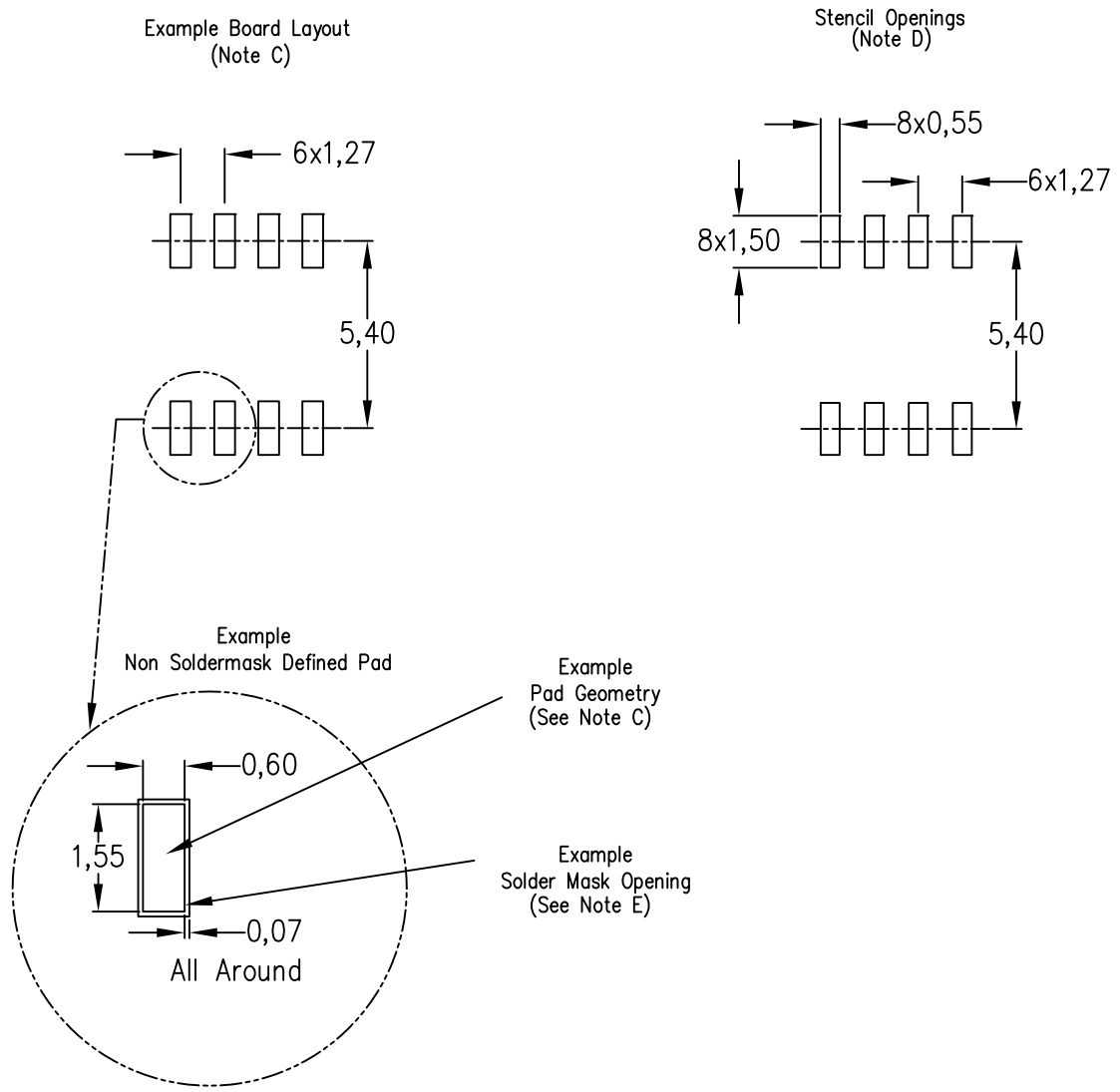
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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