ISO1050 Isolated CAN Transceiver

1 Features

- Meets the Requirements of ISO11898-2
- 5000-V_{RMS} Isolation (ISO1050DW)
- 2500-V_{RMS} Isolation (ISO1050DUB)
- Fail-Safe Outputs
- Low Loop Delay: 150 ns (Typical), 210 ns (Maximum)
- 50-kV/μs Typical Transient Immunity
- Bus-Fault Protection of –27 V to 40 V
- Driver (TXD) Dominant Time-out Function
- I/O Voltage Range Supports 3.3-V and 5-V Microprocessors
- VDE Approval per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1
- UL 1577 Approved
- CSA Approved for IEC 60950-1, IEC 61010-1, IEC 60601-1 3rd Ed (Medical) and Component Acceptance Notice 5A
- TUV 5-KV_{RMS} Reinforced Insulation Approval for EN/UL/CSA 60950-1 (ISO1050DW-Only)
- CQC Reinforced Insulation per GB4843.1-2011 (ISO1050DW-Only)
- Typical 25-Year Life at Rated Working Voltage (see Application Report SLLA197 and Figure 30)

2 Applications

- Industrial Automation, Control, Sensors, and Drive Systems
- Building and Climate Control (HVAC) Automation
- Security Systems
- Transportation
- Medical
- Telecom
- CAN Bus Standards Such as CANopen, DeviceNet, NMEA2000, ARINC825, ISO11783, CAN Kingdom, CANaerospace

3 Description

The ISO1050 is a galvanically isolated CAN transceiver that meets the specifications of the ISO11898-2 standard. The device has the logic input and output buffers separated by a silicon oxide (SiO_2) insulation barrier that provides galvanic isolation of up to 5000 V_{RMS} for ISO1050DW and 2500 V_{RMS} for ISO1050DUB. Used in conjunction with isolated power supplies, the device prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

As a CAN transceiver, the device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps). The device is designed for operation in especially harsh environments, and it features cross-wire, overvoltage and loss of ground protection from –27 V to 40 V and overtemperature shutdown, as well as –12-V to 12-V common-mode range.

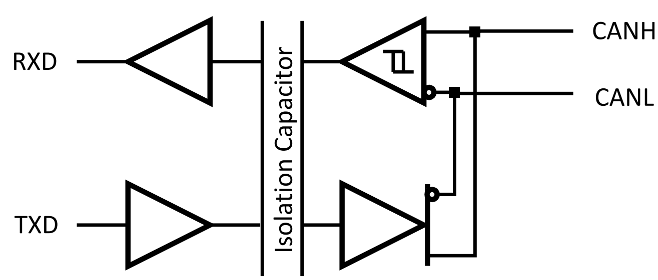
The ISO1050 is characterized for operation over the ambient temperature range of –55°C to 105°C.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO1050	SOP (8)	9.50 mm × 6.57 mm
	SOIC (16)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (June 2013) to Revision I — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision G (March 2013) to Revision H — **Page**

- Changed title From: LIFE EXPECTANCY vs WORKING VOLTAGE (ISO1050DW To: LIFE EXPECTANCY vs WORKING VOLTAGE (ISO1050DUB) 21

Changes from Revision F (January 2013) to Revision G — **Page**

- Clarified clearance and creepage measurement method in ISOLATOR CHARACTERISTICS 15
- Clarified test methods for voltage ratings in INSULATION CHARACTERISTICS 16
- Changed UL Single Protection Certification pending to Single Protection in REGULATORY INFORMATION SECTION (certificate available) 17

Changes from Revision E (December 2011) to Revision F — **Page**

- Deleted ISO1050L device 1
- Deleted ISO1050LDW from Features list 1
- Deleted ISO1050LDW in first paragraph of DESCRIPTION 1
- Added the PIN FUNCTIONS section 5
- Added Note 1 to the DRIVER SWITCHING CHARACTERISTICS table 8
- Deleted ISO1050LDW from INSULATION CHARACTERISTICS 16
- Deleted ISO1050LDW from REGULATORY INFORMATION 17
- Added the FUNCTIONAL DESCRIPTION section 17

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- Deleted ISO1050LDW from LIFE EXPECTANCY vs WORKING VOLTAGE 21
- Deleted 40V from the CANH and CANL input diagrams and output diagrams in the EQUIVALENT I/O SCHEMATICS 21
- Changed the APPLICATION INFORMATION section........ 22
- Changed the BUS LOADING, LENGHT AND NUMBER OF NODES section 22
- Added the CAN TERMINATION section 23

Changes from Revision D (June 2011) to Revision E **Page**

- Added device ISO1050L........ 1
- Changed (DW Package) in the Features list to (ISO1050DW) 1
- Changed (DUB Package) in the Features list to (ISO1050DUB and ISO1050LDW)........ 1
- Deleted IEC 60950-1 from the CSA Approvals Feature bullet 1
- From: IEC 60601-1 (Medical) and CSA Approvals Pending To: IEC 60601-1 (Medical) and CSA Approved 1
- Added Feature - 5 KVRMS Reinforced.. 1
- Changed DW Package to ISO105DW and DUB package to ISO1050DUB and ISO1050LDW in the first paragraph of DESCRIPTION 1
- Added Note 1 to the INSULATION CHARACTERISTICS table 16
- Changed V_{IORM} From: 8-DUB Package to ISO1050DUB and ISO1050LDW 16
- Changed V_{IORM} From: 16-DW to ISO1050DW 16
- Changed the V_{ISO} Isolation voltage per UL section of the INSULATION CHARACTERISTICS table. 16
- Changed the IEC 60664-1 Ratings Table 16
- Changed the REGULATORY INFORMATION table 17
- Changed in note (1) 3000 to 2500 and 6000 to 5000 17
- Changed From: File Number: 220991 (Approval Pending) To: File Number: 220991........ 17
- Changed in LIFE EXPECTANCY vs WORKING VOLTAGE (8-DUB PACKAGE TO: LIFE.....(ISO1050DW and ISO1050LDW) 21

Changes from Revision C (July 2010) to Revision D **Page**

- Changed the SUPPLY CURRENT table for I_{CC1} 1st row From: Typ = 1 To: 1.8 and MAX = 2 To: 2.8........ 7
- Changed the SUPPLY CURRENT table for I_{CC1} 2nd row From: Typ = 2 To: 2.8 and MAX = 3 To: 3.6 7
- Changed the REGULATORY INFORMATION table 17

Changes from Revision B (June 2009) to Revision C **Page**

- Changed the IEC 60747-5-2 Features bullet From: DW package Approval Pending To: VDE approved for both DUB and DW packages 1
- Changed the Minimum Internal Gap value from 0.008 to 0.014 in the Isolator Characteristics table........ 15
- Changed V_{IORM} Specification From: 1300 To: 1200 per VDE certification 16
- Changed V_{PR} Specification From 2438 To: 2250 16
- Added the Bus Loading paragraph to the Application Information section 22

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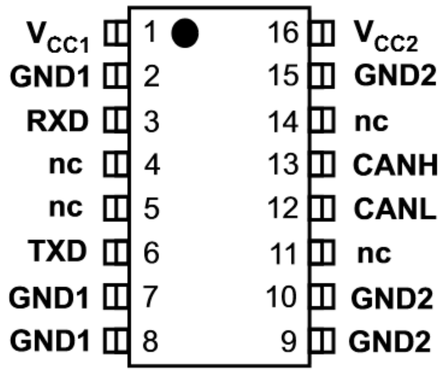
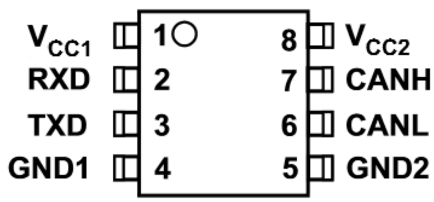
5 Pin Configuration and Functions

16-Pin
DW Package
Top View



8-Pin
DUB Package
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DW	DUB		
V_{CC1}	1	1	Supply	Digital-side supply voltage (3 to 5.5 V)
GND1	2	—	Ground	Digital-side ground connection
RXD	3	2	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
NC	4	—	NC	No connect
NC	5	—	NC	No connect
TXD	6	3	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
GND1	7	4	Ground	Digital-side ground connection
GND1	8	—	Ground	Digital-side ground connection
GND2	9	5	Ground	Transceiver-side ground connection
GND2	10	—	Ground	Transceiver-side ground connection
NC	11	—	NC	No connect
CANL	12	6	I/O	Low-level CAN bus line
CANH	13	7	I/O	High-level CAN bus line
NC	14	—	NC	No connect
GND2	15	—	Ground	Transceiver-side ground connection
V_{CC2}	16	8	Supply	Transceiver-side supply voltage (5 V)

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6 Specifications

6.1 Absolute Maximum Ratings[1][2]

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage [3]	–0.5	6	V
V_I	Voltage input (TXD)	–0.5	V_{CC1}+ 0.5[4]	V
V_{CANH} or V_{CANL}	Voltage at any bus terminal (CANH, CANL)	–27	40	V
I_O	Receiver output current	–15	15	mA
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This isolator is suitable for isolation within the safety limiting data. Maintenance of the safety data must be ensured by means of protective circuitry.
(3) All input and output logic voltage values are measured with respect to the GND1 logic side ground. Differential bus-side voltages are measured to the respective bus-side GND2 ground terminal.
(4) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1500	
		Machine model, ANSI/ESDS5.2-1996, all pins	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage, controller side		3		5.5	V
V_{CC2}	Supply voltage, bus side		4.75	5	5.25	V
V_I or V_{IC}	Voltage at bus pins (separately or common mode)		–12[1]		12	V
V_{IH}	High-level input voltage	TXD	2		5.25	V
V_{IL}	Low-level input voltage	TXD	0		0.8	V
V_{ID}	Differential input voltage		–7		7	V
I_{OH}	High-level output current	Driver	–70			mA
		Receiver	–4			
I_{OL}	Low-level output current	Driver			70	mA
		Receiver			4	
T_A	Ambient Temperature		–55		105	°C
T_J	Junction temperature (see *Thermal Information*)		–55		125	°C
P_D	Total power dissipation	V_{CC1}= 5.5V, V_{CC2}= 5.25V, T_A=105°C, R_L= 60Ω, TXD input is a 500kHz 50% duty-cycle square wave			200	mW
P_{D1}	Power dissipation by Side-1				25	
P_{D2}	Power dissipation by Side-2				175	
$T_{j\ shutdown}$	Thermal shutdown temperature[2]			190		°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) Extended operation in thermal shutdown may affect device reliability.

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6.4 Thermal Information

THERMAL METRIC(1)		ISO1050 DW 16 PINS	ISO1050 DUB 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.0	73.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41	63.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.7	43.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.4	27.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.2	42.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: Supply Current

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC1}	V_{CC1} Supply current		V_I = 0 V or V_{CC1} , V_{CC1} = 3.3V		1.8	2.8	mA
			V_I = 0 V or V_{CC1} , V_{CC1} = 5V		2.3	3.6	
I_{CC2}	V_{CC2} Supply current	Dominant	V_I = 0 V, 60-Ω Load		52	73	mA
		Recessive	V_I = V_{CC1}		8	12	

(1) All typical values are at 25°C with V_{CC1} = V_{CC2} = 5 V.

6.6 Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	See Figure 7 and Figure 8, V_I = 0 V, R_L = 60 Ω	2.9	3.5	4.5	V
		CANL		0.8	1.2	1.5	
$V_{O(R)}$	Bus output voltage (Recessive)		See Figure 7 and Figure 8, V_I = 2 V, R_L= 60 Ω	2	2.3	3	V
$V_{OD(D)}$	Differential output voltage (Dominant)		See Figure 7, Figure 8 and Figure 9, V_I = 0 V, R_L = 60 Ω	1.5		3	V
			See Figure 7, Figure 8, and Figure 9 V_I = 0 V, R_L = 45Ω, Vcc > 4.8 V	1.4		3	
$V_{OD(R)}$	Differential output voltage (Recessive)		See Figure 7 and Figure 8, V_I = 3 V, R_L = 60 Ω	–0.12		0.012	V
			V_I = 3 V, No Load	–0.5		0.05	
$V_{OC(D)}$	Common-mode output voltage (Dominant)		See Figure 14	2	2.3	3	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage				0.3		
I_{IH}	High-level input current, TXD input		V_I at 2 V			5	μA
I_{IL}	Low-level input current, TXD input		V_I at 0.8 V	–5			μA
$I_{O(off)}$	Power-off TXD leakage current		V_{CC1}, V_{CC2} at 0 V, TXD at 5 V			10	μA
$I_{OS(ss)}$	Short-circuit steady-state output current		See Figure 17, V_{CANH} = –12 V, CANL Open	–105	–72		mA
			See Figure 17, V_{CANH} = 12 V, CANL Open		0.36	1	
			See Figure 17, V_{CANL} =–12 V, CANH Open	–1	–0.5		
			See Figure 17, V_{CANL} = 12 V, CANH Open		71	105	
C_O	Output capacitance		See receiver input capacitance				
CMTI	Common-mode transient immunity		See Figure 19, V_I = V_{CC} or 0 V	25	50		kV/μs

6.7 Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going bus input threshold voltage	See Table 1		750	900	mV
V_{IT-}	Negative-going bus input threshold voltage		500	650		mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			150		mV
V_{OH}	High-level output voltage with Vcc = 5 V	I_{OH} = –4 mA, See Figure 12	V_{CC} – 0.8	4.6		V
		I_{OH} = –20 µA, See Figure 12	V_{CC} – 0.1	5		
V_{OH}	High-level output voltage with Vcc1 = 3.3 V	I_{OL} = 4 mA, See Figure 12	V_{CC} – 0.8	3.1		V
		I_{OL} = 20 µA, See Figure 12	V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 12		0.2	0.4	V
		I_{OL} = 20 µA, See Figure 12		0	0.1	
C_I	Input capacitance to ground, (CANH or CANL)	TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5 V		6		pF
C_{ID}	Differential input capacitance	TXD at 3 V, V_I = 0.4 sin (4E6πt)		3		pF
R_{ID}	Differential input resistance	TXD at 3 V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)	TXD at 3 V	15	30	40	kΩ
$R_{I(m)}$	Input resistance matching (1 – [$R_{IN (CANH)}$ / $R_{IN (CANL)}$]) × 100%	$V_{CANH} = V_{CANL}$	–3%	0%	3%	
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See Figure 19	25	50		kV/µs

(1) All typical values are at 25°C with $V_{CC1} = V_{CC2}$ = 5 V.

6.8 Switching Characteristics: Device

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{loop1}	Total loop delay, driver input to receiver output, Recessive to Dominant	See Figure 15	112	150	210	ns
t_{loop2}	Total loop delay, driver input to receiver output, Dominant to Recessive	See Figure 15	112	150	210	ns

6.9 Switching Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, recessive-to-dominant output	See Figure 10	31	74	110	ns
t_{PHL}	Propagation delay time, dominant-to-recessive output		25	44	75	
t_r	Differential output signal rise time			20	50	
t_f	Differential output signal fall time			20	50	
t_{TXD_DTO}(1)	Dominant time-out	↓ C_L=100 pF, See Figure 16	300	450	700	µs

(1) The TXD dominant time out (t_{TXD_DTO}) disables the driver of the transceiver once the TXD has been dominant longer than (t_{TXD_DTO}) which releases the bus lines to recessive preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults locking the bus dominant it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case where five successive dominant bits are followed immediately by an error frame. This along with the (t_{TXD_DTO}) minimum limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11/ (t_{TXD_DTO}) = 11 bits / 300 µs = 37 kbps.

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6.10 Switching Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	TXD at 3 V, See Figure 12	66	90	130	ns
t_{PHL}	Propagation delay time, high-to-low-level output		51	80	105	
t_r	Output signal rise time			3	6	
t_f	Output signal fall time			3	6	
t_{fs}	Fail-Safe output delay time from bus-side power loss	VCC1 at 5 V, See Figure 18		6		μs

6.11 Typical Characteristics

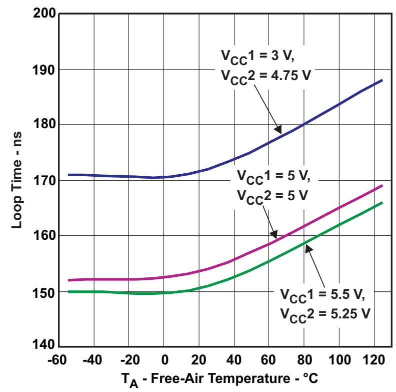

Figure 1. Recessive-to-Dominant Loop Time vs Free-Air Temperature (Across Vcc)

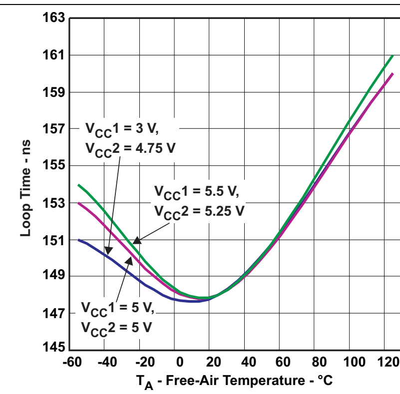

Figure 2. Dominant-to-Recessive Loop Time vs Free-Air Temperature (Across Vcc)

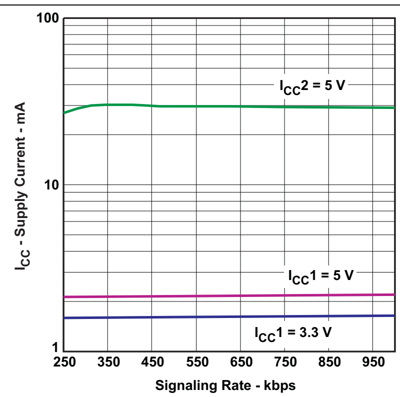

Figure 3. Supply Current (RMS) vs Signaling Rate (kbps)

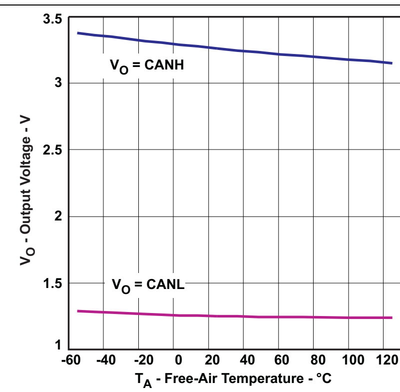

Figure 4. Driver Output Voltage vs Free-Air Temperature

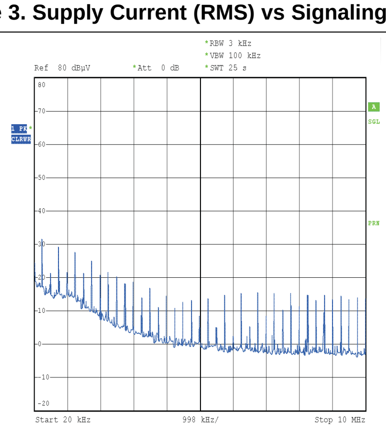

Figure 5. Emissions Spectrum to 10 MHz

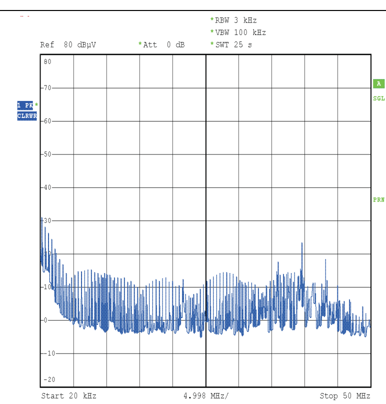

Figure 6. Emissions Spectrum to 50 MHz

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7 Parameter Measurement Information

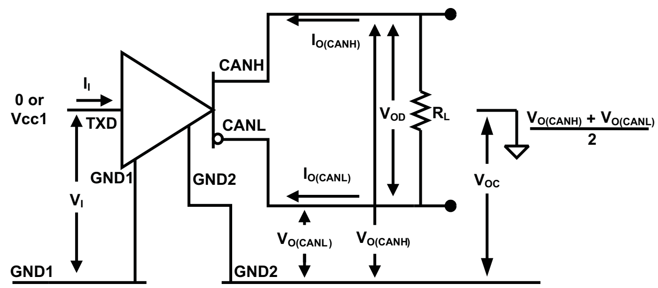


Figure 7. Driver Voltage, Current and Test Definitions

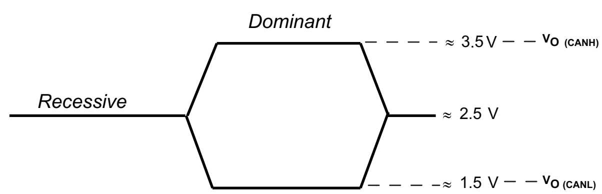


Figure 8. Bus Logic State Voltage Definitions

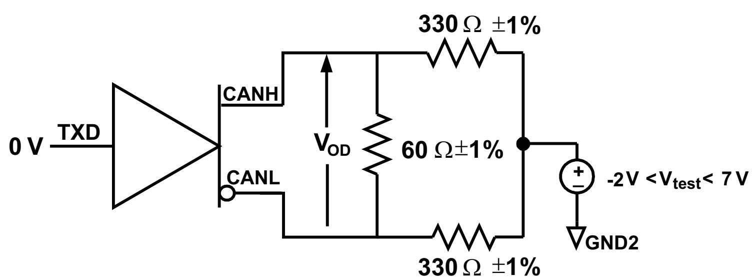
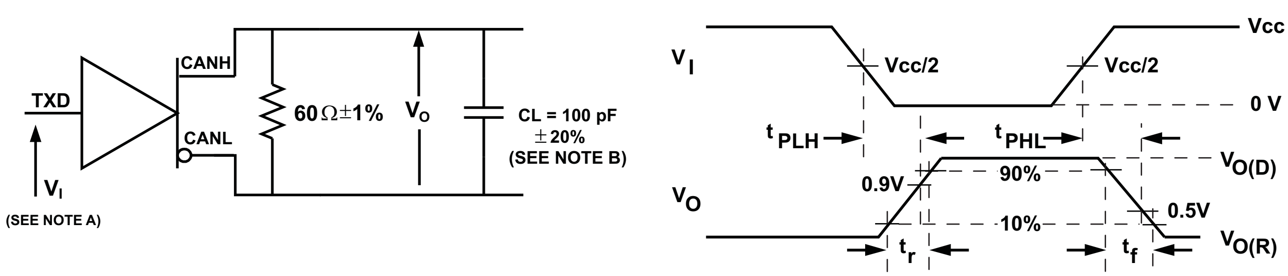


Figure 9. Driver V_{OD} With Common-Mode Loading Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 10. Driver Test Circuit and Voltage Waveforms

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Parameter Measurement Information (continued)

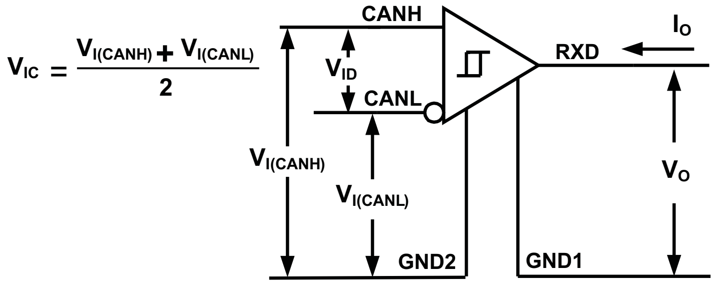
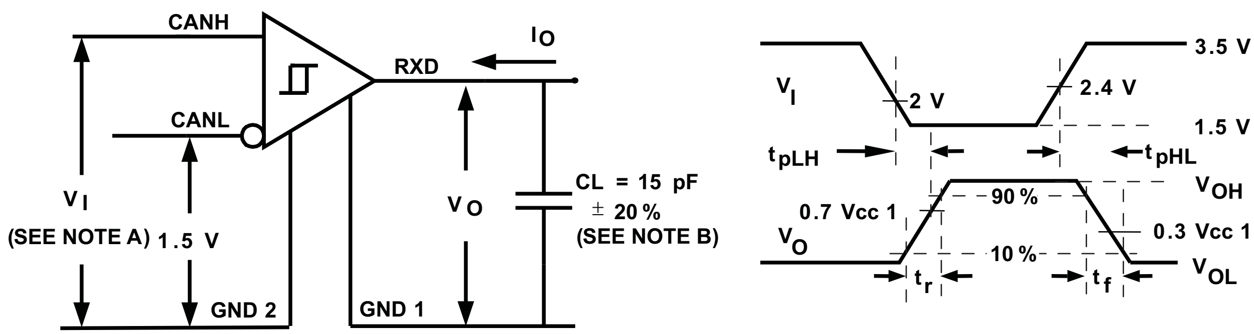


Figure 11. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 12. Receiver Test Circuit and Voltage Waveforms

Table 1. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\|V_{ID}\|$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	–6 V	H	
6 V	12 V	–6 V	H	
Open	Open	X	H	

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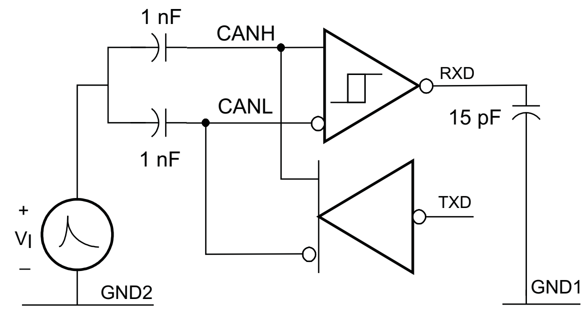

Figure 13. Transient Overvoltage Test Circuit

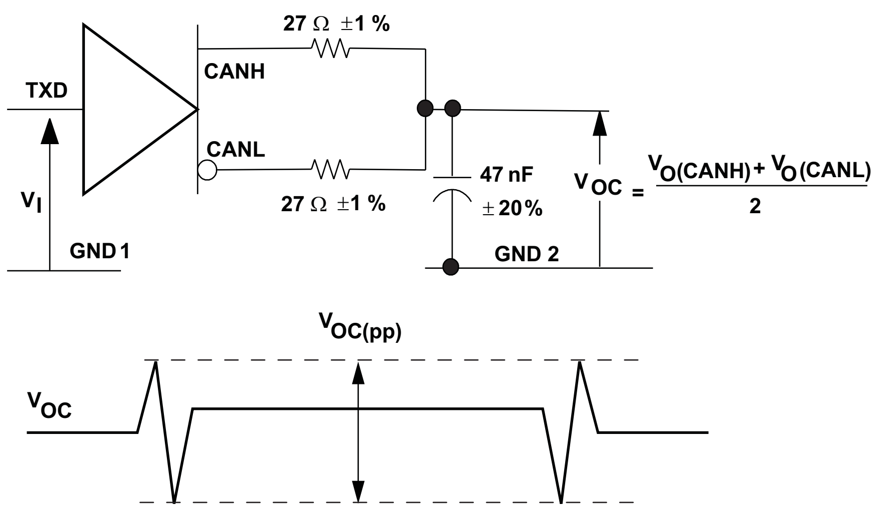

Figure 14. Peak-to-Peak Output Voltage Test Circuit and Waveform

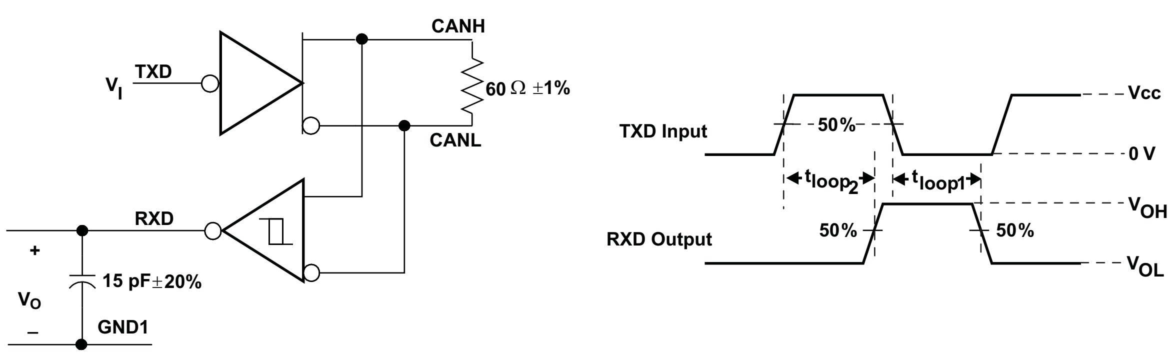

Figure 15. t_{LOOP} Test Circuit and Voltage Waveforms

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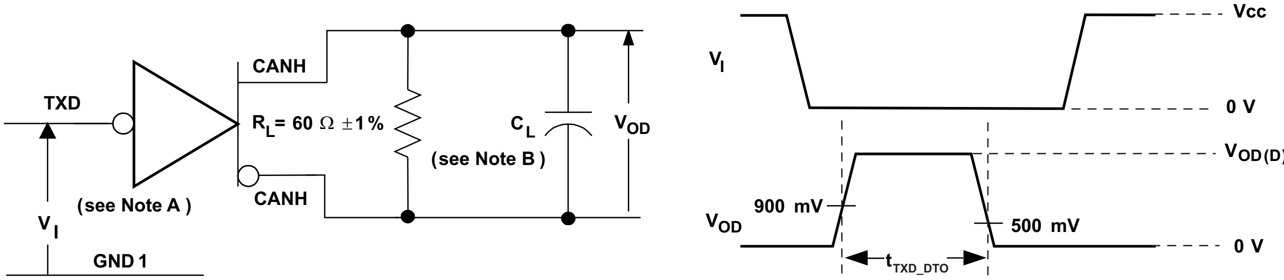

A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 16. Dominant Time-out Test Circuit and Voltage Waveforms

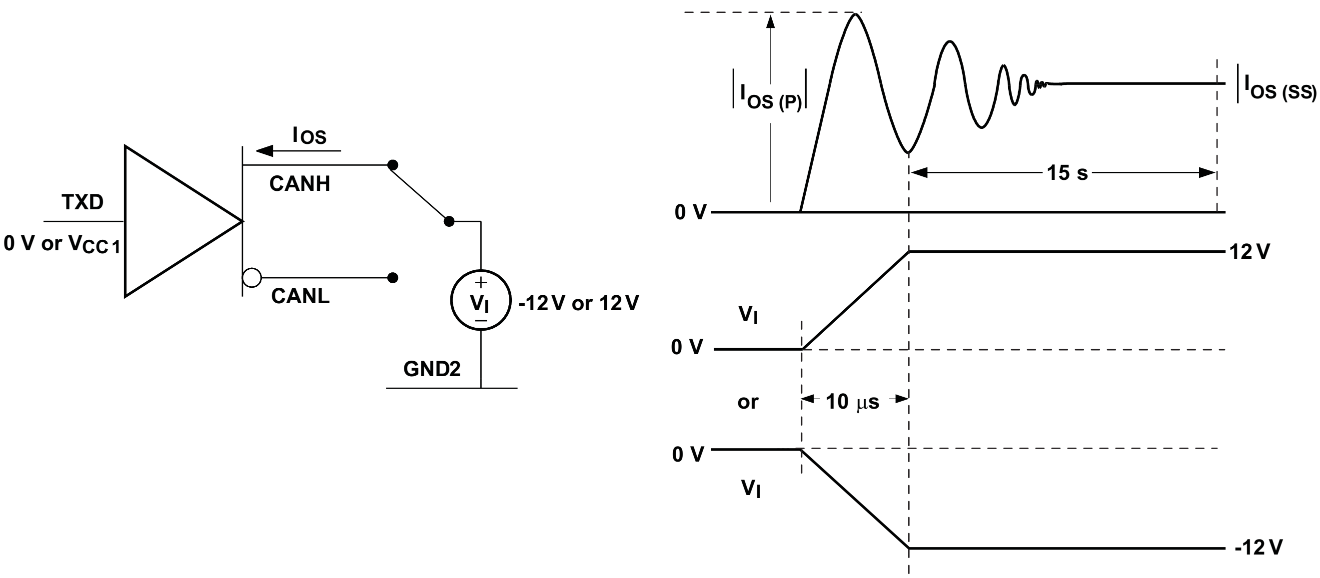

Figure 17. Driver Short-Circuit Current Test Circuit and Waveforms

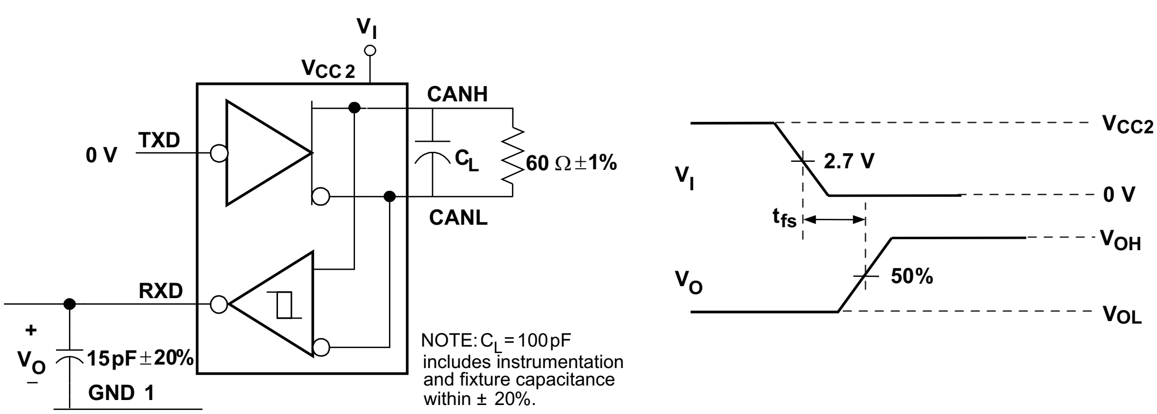

Figure 18. Fail-Safe Delay Time Test Circuit and Voltage Waveforms

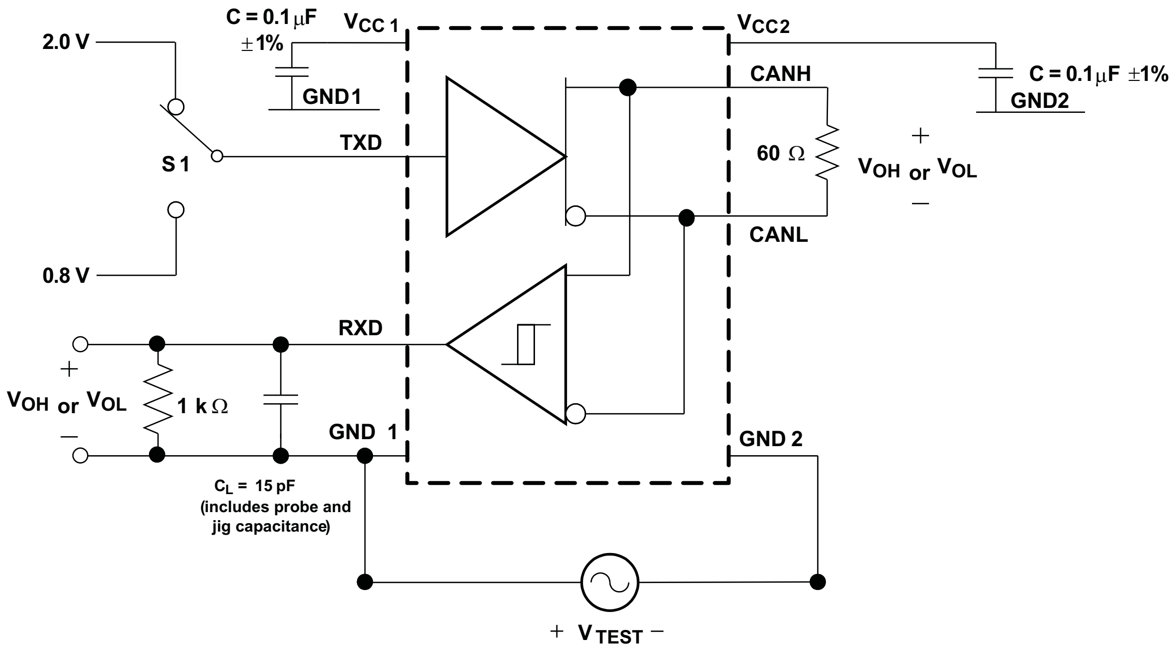

Figure 19. Common-Mode Transient Immunity Test Circuit

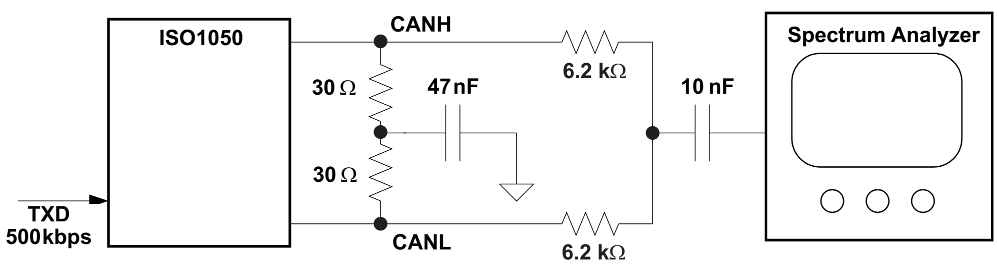

Figure 20. Electromagnetic Emissions Measurement Setup

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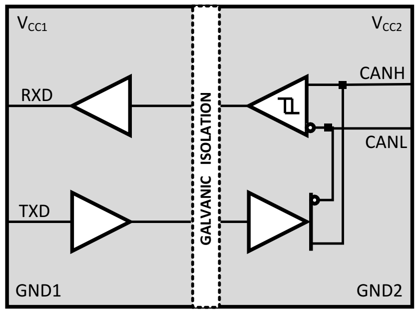
8 Detailed Description

8.1 Overview

The ISO1050 is a digitally isolated CAN transceiver with a typical transient immunity of 50 kV/µs. The device can operate from 3.3-V supply on side 1 and 5-V supply on side 2. This is of particular advantage for applications operating in harsh industrial environments because the 3.3 V on side 1 enables the connection to low-volt microcontrollers for power preservation, whereas the 5 V on side 2 maintains a high signal-to-noise ratio of the bus signals.

8.2 Functional Block Diagram



8.3 Feature Description

Table 2. Isolator Characteristics(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest pin-to-pin distance through air, per JEDEC package dimensions	DUB-8	6.1			mm
L(I02)	Minimum external tracking (Creepage)	Shortest pin-to-pin distance across the package surface, per JEDEC package dimensions	DUB-8	6.8			mm
L(I01)	Minimum air gap (Clearance)	Shortest pin-to-pin distance through air, per JEDEC package dimensions	DW-16	8.34			mm
L(I02)	Minimum external tracking (Creepage)	Shortest pin-to-pin distance across the package surface, per JEDEC package dimensions	DW-16	8.10			mm
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation		0.014			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-pin device, T_A = 25°C			$>10^{12}$		Ω
		Input to output, V_{IO} = 500 V, 100°C ≤ T_A ≤ T_A max			$>10^{11}$		Ω
C_{IO}	Barrier capacitance	V_I = 0.4 sin (4E6πt)			1.9		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)			1.3		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit-board do not reduce this distance.
(2) Creepage and clearance on a printed-circuit-board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed-circuit-board are used to help increase these specifications.

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Table 3. Insulation Characteristics

PARAMETER			TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	ISO1050DUB		560	Vpeak
		ISO1050DW		1200	
V_{PR}	Input to output test voltage per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	ISO1050DUB	V_{PR} = 1.875 x V_{IORM}, t = 1 sec (100% production) Partial discharge < 5 pC	1050	Vpeak
		ISO1050DW		2250	
V_{IOTM}	Transient overvoltage per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12		t = 60 sec (qualification)	4000	Vpeak
			t = 1 sec (100% production)		
V_{ISO}	Isolation voltage per UL 1577	ISO1050DUB - Double Protection	t = 60 sec (qualification)	2500	Vrms
			t = 1 sec (100% production)	3000	
		ISO1050DW - Single Protection	t = 60 sec (qualification)	4243	Vrms
			t = 1 sec (100% production)	5092	
R_S	Isolation resistance		V_{IO} = 500 V at T_S	> 10^9	Ω
	Pollution Degree			2	

Table 4. IEC 60664-1 Ratings

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 Vrms	I–IV
	Rated mains voltage ≤ 300 Vrms	I–III
	Rated mains voltage ≤ 400 Vrms	I–II
	Rated mains voltage ≤ 600 Vrms (ISO1050DW only)	I-II
	Rated mains voltage ≤ 848 Vrms (ISO1050DW only)	I

Table 5. IEC Safety Limiting Values(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DUB-8	θ_{JA} = 73.3 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			310	mA
			θ_{JA} = 73.3 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			474	
		DW-16	θ_{JA} = 76 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			299	mA
			θ_{JA} = 76 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			457	
T_S	Maximum case temperature					150	°C

(1) Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assured junction-to-air thermal resistance in *Thermal Information* is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

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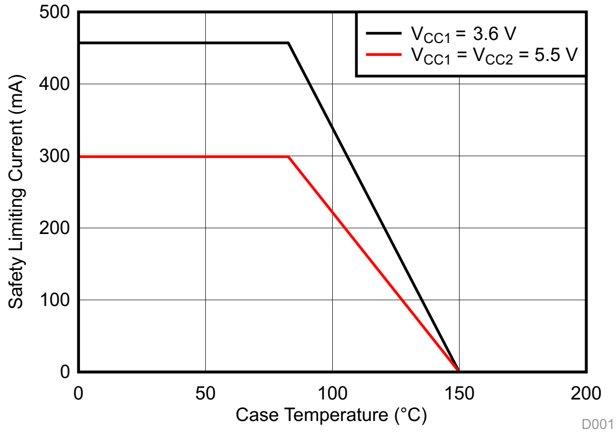

Figure 21. DUB-8 θ_{JC} Thermal Derating Curve per VDE

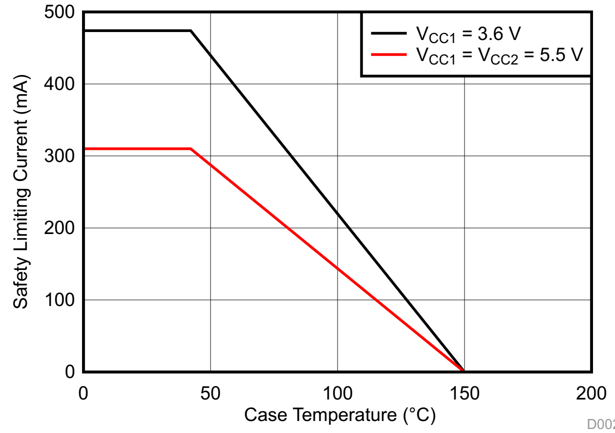

Figure 22. DW-16 θ_{JC} Thermal Derating Curve per VDE

Table 6. Regulatory Information

VDE	TUV	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 & DIN EN 61010-1	Certified according to EN/UL/CSA 60950-1	Approved under CSA Component Acceptance Notice 5A	Recognized under 1577 Component Recognition Program(1)	Certified according to GB4943.1-2011
Basic Insulation Transient Overvoltage, 4000 V_{PK} Surge Voltage, 4000 V_{PK} Maximum Working Voltage, 1200 V_{PK} (ISO1050DW) and 560 V_{PK} (ISO1050DUB)	**ISO1050DW:** 5000 V_{RMS} Reinforced Insulation, 400 V_{RMS} maximum working voltage 5000 V_{RMS} Basic Insulation, 600 V_{RMS} maximum working voltage **ISO1050DUB:** 2500 V_{RMS} Reinforced Insulation, 400 V_{RMS} maximum working voltage 2500 V_{RMS} Basic Insulation, 600 V_{RMS} maximum working voltage	5000 V_{RMS} Reinforced Insulation 2 Means of Patient Protection at 125 V_{RMS} per IEC 60601-1 (3rd Ed.)	ISO1050DUB: 2500 V_{RMS} Double Protection ISO1050DW: 3500 V_{RMS} Double Protection, 4243 V_{RMS} Single Protection	**ISO1050DW:** Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40016131	Certificate number: U8V 11 09 77311 008	Master contract number: 220991	File number: E181974	Certificate number: CQC14001109541

(1) Production tested ≥ 3000 V_{RMS} (ISO1050DUB) and 5092 V_{RMS} (ISO1050DW) for 1 second in accordance with UL 1577.

8.3.1 CAN Bus States

The CAN bus has two states during operation: *dominant* and *recessive*. A dominant bus state, equivalent to logic low, is when the bus is driven differentially by a driver. A recessive bus state is when the bus is biased to a common mode of V_{CC} / 2 through the high-resistance internal input resistors of the receiver, equivalent to a logic high. The host microprocessor of the CAN node will use the TXD pin to drive the bus and will receive data from the bus on the RXD pin. See Figure 23 and Figure 24.

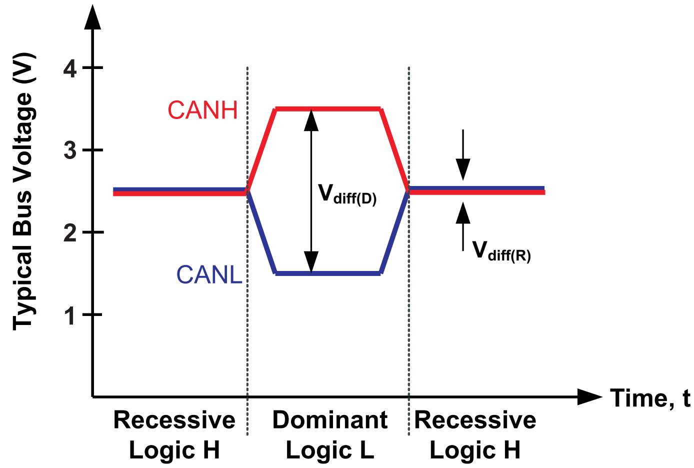

Figure 23. Bus States (Physical Bit Representation)

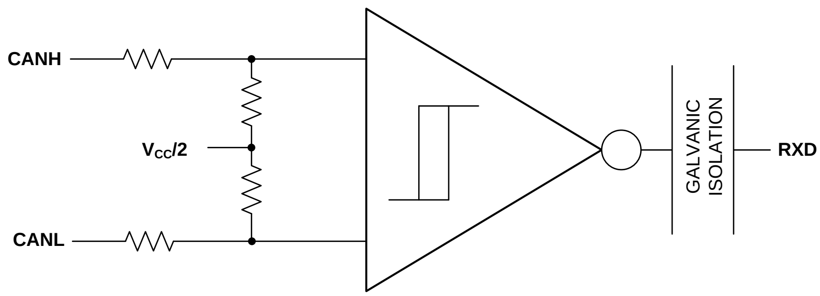

Figure 24. Simplified Recessive Common Mode Bias and Receiver

8.3.2 Digital Inputs and Outputs

TXD (Input) and RXD (Output):

V_{CC1} for the isolated digital input and output side of the device maybe supplied by a 3.3-V or 5-V supply and thus the digital inputs and outputs are 3.3-V and 5-V compatible.

NOTE

TXD is very weakly internally pulled up to V_{CC1}. An external pullup resistor should be used to make sure that TXD is biased to recessive (high) level to avoid issues on the bus if the microprocessor doesn't control the pin and TXD floats. TXD pullup strength and CAN bit timing require special consideration when the device is used with an open-drain TXD output on the CAN controller of the microprocessor. An adequate external pullup resistor must be used to ensure that the TXD output of the microprocessor maintains adequate bit timing input to the input on the transceiver.

8.3.3 Protection Features

8.3.3.1 TXD Dominant Time-Out (DTO)

TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the time-out period t_{TXD_DTO}. The TXD DTO circuit timer starts on a falling edge on TXD. The TXD DTO circuit disables the CAN bus driver if no rising edge is seen before the time-out period expires. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on the TXD pin, thus clearing the TXD DTO condition. The receiver and RXD pin still reflect the CAN bus, and the bus pins are biased to recessive level during a TXD dominant time-out.

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NOTE

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum data rate. Calculate the minimum transmitted data rate by: Minimum Data Rate = 11 / t_{TXD_DTO}.

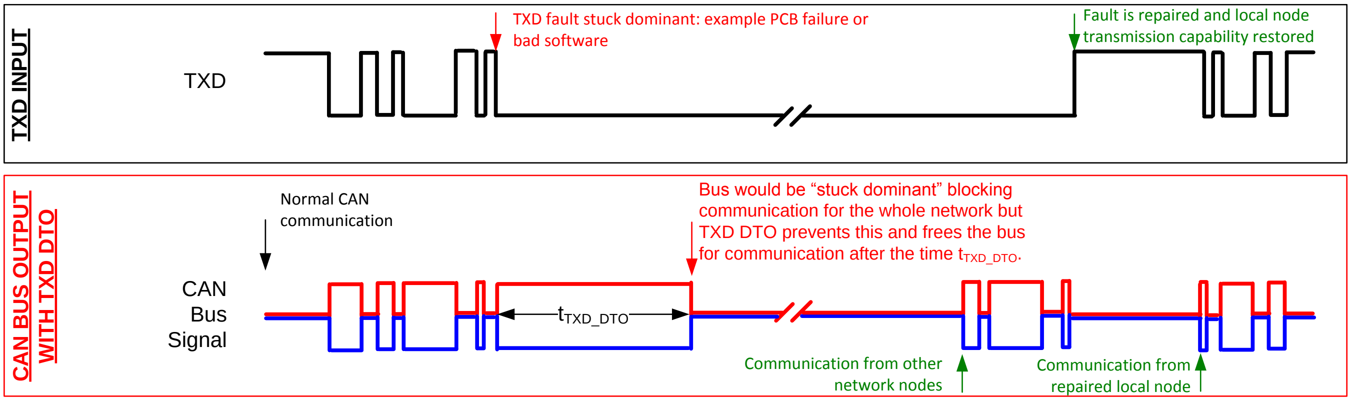

Figure 25. Example Timing Diagram for Devices With TXD DTO

8.3.3.2 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shut down threshold the device turns off the CAN driver circuits thus blocking the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature drops below the thermal shutdown temperature of the device. If the fault condition is still present, the temperature may rise again and the device would enter thermal shut down again. Prolonged operation with thermal shutdown conditions may affect device reliability.

NOTE

During thermal shutdown the CAN bus drivers turn off; thus no transmission is possible from TXD to the bus. The CAN bus pins are biased to recessive level during a thermal shutdown, and the receiver to RXD path remains operational.

8.3.3.3 Undervoltage Lockout and Fail-Safe

The supply pins have undervoltage detection that places the device in protected or fail-safe mode. This protects the bus during an undervoltage event on V_{CC1} or V_{CC2} supply pins. If the bus-side power supply Vcc2 is lower than about 2.7V, the power shutdown circuits in the ISO1050 will disable the transceiver to prevent false transmissions due to an unstable supply. If Vcc1 is still active when this occurs, the receiver output (RXD) will go to a fail-safe HIGH (recessive) value in about 6 microseconds.

Table 7. Undervoltage Lockout and Fail-Safe

$V_{CC}1$	$V_{CC}2$	DEVICE STATE	BUS OUTPUT	RXD
GOOD	GOOD	Functional	Per Device State and TXD	Mirrors Bus
BAD	GOOD	Protected	Recessive	High Impedance (3-state)
GOOD	BAD	Protected	High Impedance	Recessive (Fail-Safe High)

NOTE

After an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically resumes normal operation in 300 µs

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8.3.3.4 Floating Pins

Pullups and pulldowns should be used on critical pins to place the device into known states if the pins float. The TXD pin should be pulled up through a resistor to V_{CC1} to force a recessive input level if the microprocessor output to the pin floats.

8.3.3.5 CAN Bus Short-Circuit Current Limiting

The device has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include driver current limiting (dominant and recessive). The device has TXD dominant state time out to prevent permanent higher short-circuit current of the dominant state during a system fault. During CAN communication the bus switches between dominant and recessive states with the data and control fields bits, thus the short-circuit current may be viewed either as the instantaneous current during each bus state, or as a DC average current. For system current (power supply) and power considerations in the termination resistors and common-mode choke ratings, use the average short-circuit current. Determine the ratio of dominant and recessive bits by the data in the CAN frame plus the following factors of the protocol and PHY that force either recessive or dominant at certain times:

- Control fields with set bits
- Bit-stuffing
- Interframe space
- TXD dominant time-out (fault case limiting)

These ensure a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

NOTE

The short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated with the following formula:

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times I_{OS(SS)\_REC}) + (\%DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%Receive \times I_{OS(SS)\_REC}]$$

Where

- $I_{OS(AVG)}$ is the average short-circuit current.
- %Transmit is the percentage the node is transmitting CAN messages.
- %Receive is the percentage the node is receiving CAN messages.
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages.
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages.
- $I_{OS(SS)\_REC}$ is the recessive steady state short-circuit current.
- $I_{OS(SS)\_DOM}$ is the dominant steady state short-circuit current.

NOTE

Consider the short.circuit current and possible fault cases of the network when sizing the power ratings of the termination resistance and other network components.

8.4 Device Functional Modes

Table 8. Driver Function Table

INPUT	OUTPUTS		DRIVEN BUS STATE
TXD(1)	CANH(1)	CANL(1)	
L	H	L	Dominant
H	Z	Z	Recessive

(1) H = high level, L = low level, Z = common mode (recessive) bias to V_{CC} / 2. See Figure 23 and Figure 24 for bus state and common mode bias information.

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Table 9. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$	BUS STATE	RXD PIN(1)
Normal or Silent	$V_{ID} \geq 0.9$ V	Dominant	L
	$0.5\text{ V} < V_{ID} < 0.9\text{ V}$	?	?
	$V_{ID} \leq 0.5$ V	Recessive	H
	Open ($V_{ID} \approx 0$ V)	Open	H

(1) H = high level, L = low level, ? = indeterminate.

Table 10. Function Table(1)

DRIVER				RECEIVER		
INPUTS	OUTPUTS		BUS STATE	DIFFERENTIAL INPUTS V_{ID} = CANH–CANL	OUTPUT RXD	BUS STATE
TXD	CANH	CANL				
L(2)	H	L	DOMINANT	$V_{ID} \geq 0.9$ V	L	DOMINANT
H	Z	Z	RECESSIVE	$0.5\text{ V} < V_{ID} < 0.9\text{ V}$	?	?
Open	Z	Z	RECESSIVE	$V_{ID} \leq 0.5$ V	H	RECESSIVE
X	Z	Z	RECESSIVE	Open	H	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance
(2) Logic low pulses to prevent dominant time-out.

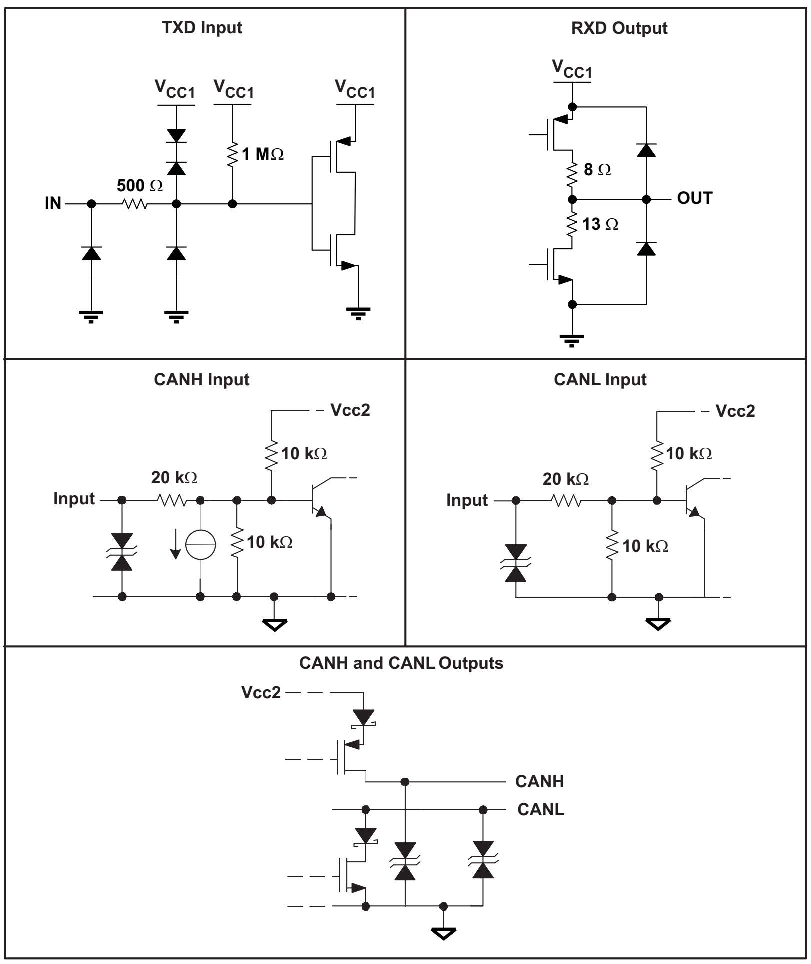

Figure 26. Equivalent I/O Schematics

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

ISO1050 can be used with other components from TI such as a microcontroller, a transformer driver, and a linear voltage regulator to form a fully isolated CAN interface.

9.2 Typical Application

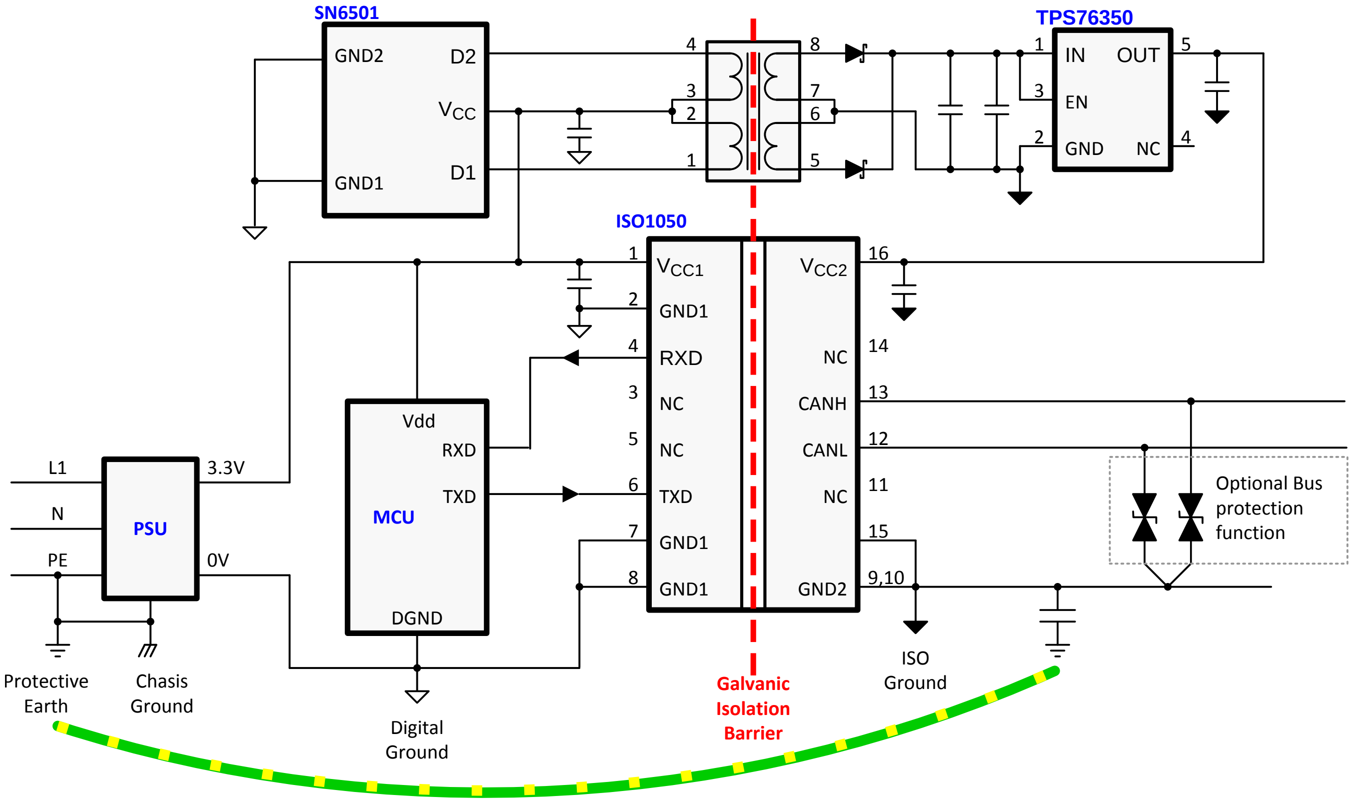

Figure 27. Application Circuit

9.2.1 Design Requirements

Unlike optocoupler-based solution, which needs several external components to improve performance, provide bias, or limit current, ISO1050 only needs two external bypass capacitors to operate.

9.2.2 Detailed Design Procedure

9.2.2.1 Bus Loading, Length and Number of Nodes

The ISO11898 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the ISO1050.

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Typical Application (continued)

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898 standard. They have made system level trade offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, CAN Kingdom, DeviceNet and NMEA200.

A CAN network design is a series of tradeoffs, but these devices operate over wide –12-V to 12-V common-mode range. In ISO11898-2 the driver differential output is specified with a 60-Ω load (the two 120-Ω termination resistors in parallel) and the differential output must be greater than 1.5 V. The ISO1050 is specified to meet the 1.5-V requirement with a 60-Ω load, and additionally specified with a differential output of 1.4 V with a 45-Ω load. The differential input resistance of the ISO1050 is a minimum of 30 kΩ. If 167 ISO1050 transceivers are in parallel on a bus, this is equivalent to a 180-Ω differential load. That transceiver load of 180 Ω in parallel with the 60 Ω gives a total 45 Ω. Therefore, the ISO1050 theoretically supports over 167 transceivers on a single bus segment with margin to the 1.2-V minimum differential input at each node. However for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO11898 standard of 40 m by careful system design and data rate tradeoffs. For example, CAN open network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO11898 CAN standard. In using this flexibility comes the responsibility of good network design.

9.2.2.2 CAN Termination

The ISO11898 standard specifies the interconnect to be a single twisted pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that it is not removed from the bus.

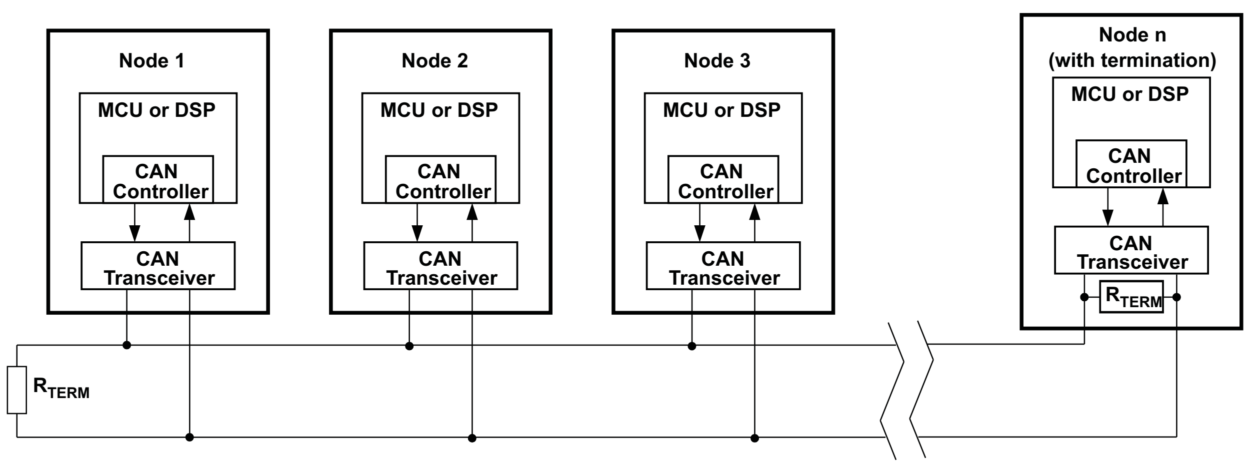

Figure 28. Typical CAN Bus

Termination may be a single 120-Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. (See Figure 29). Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

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Typical Application (continued)

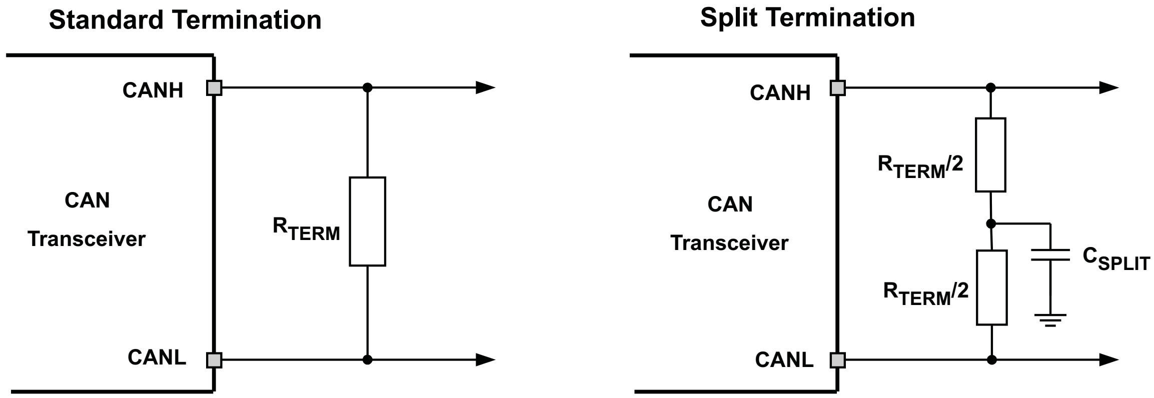

Figure 29. CAN Bus Termination Concepts

9.2.3 Application Curve

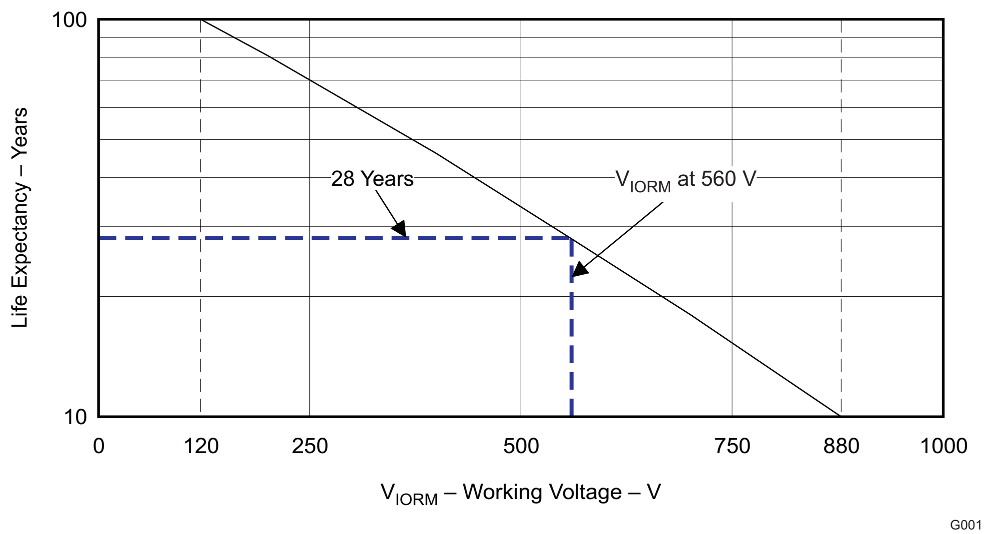

Figure 30. Life Expectancy vs Working Voltage (ISO1050DUB)

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10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as TI's SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 31). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

11.2 Layout Example

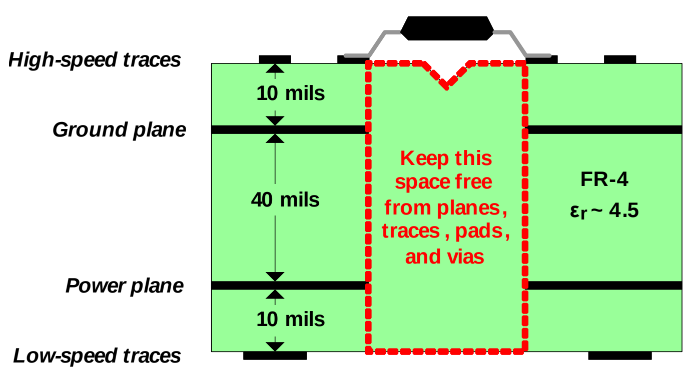

Figure 31. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- *High-Voltage Lifetime of the ISO72x Family of Digital Isolators* (SLLA197)
- *Transformer Driver for Isolated Power Supplies* (SLLSEA0)
- *Digital Isolator Design Guide* (SLLA284)

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

SLLA353 -- *Isolation Glossary.*

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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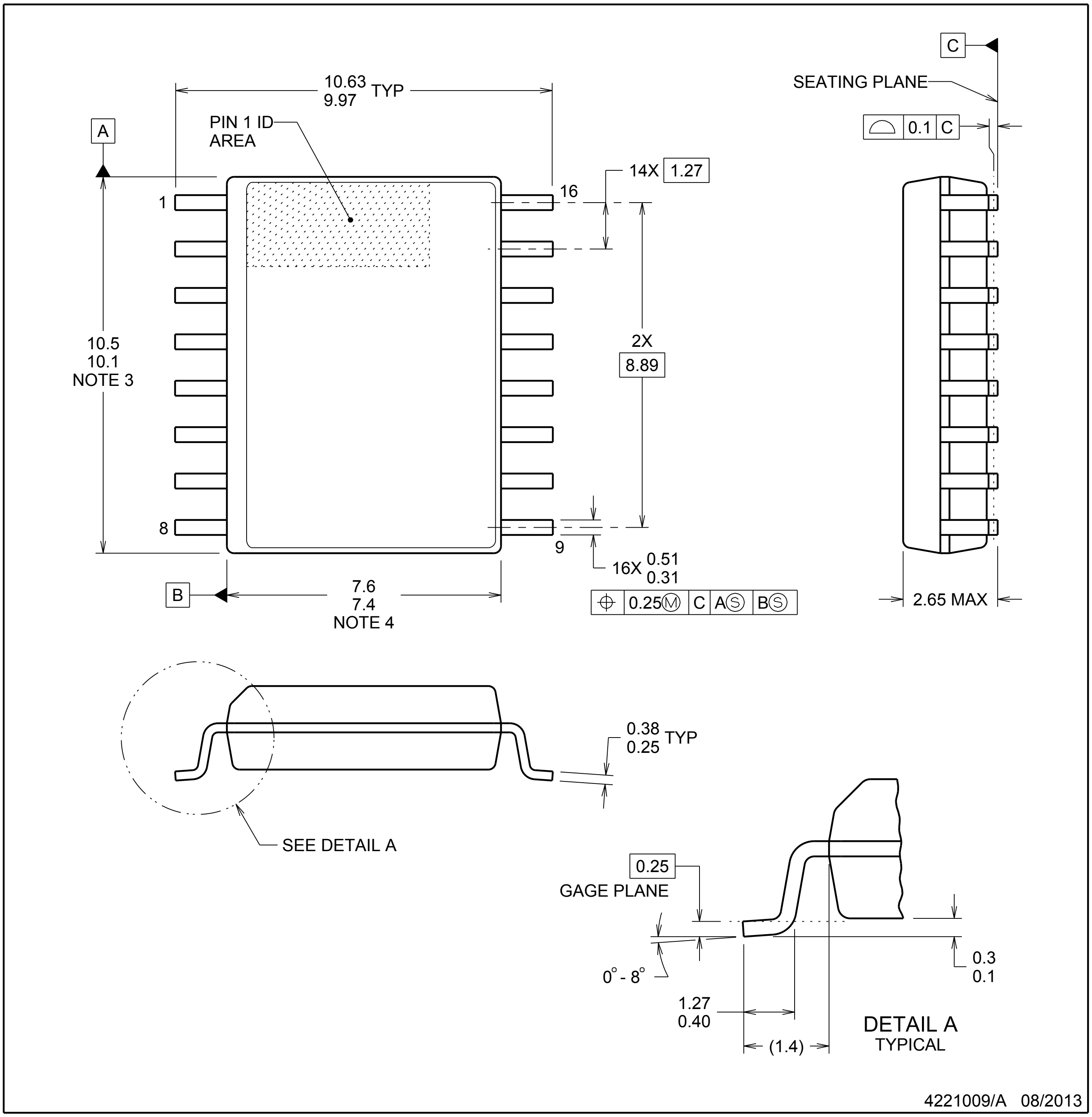
DW0016B

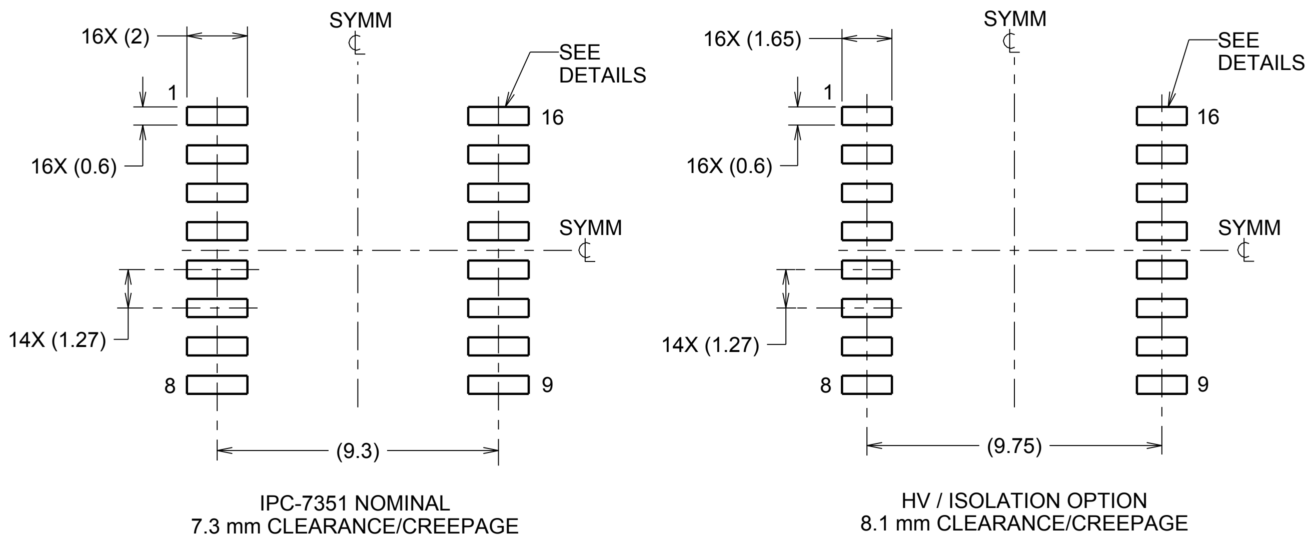
SOIC - 2.65 mm max height

SOIC

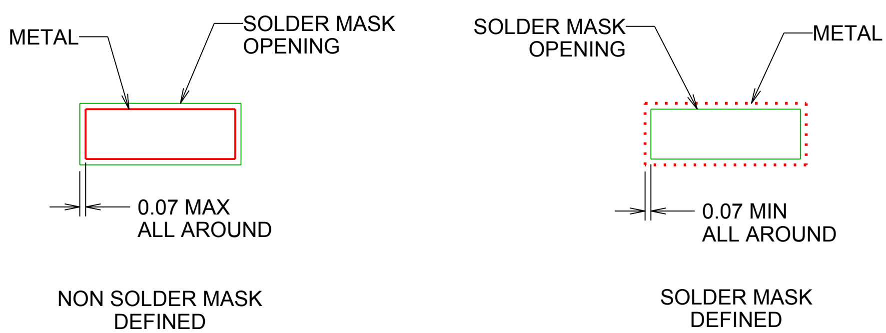


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-013, variation AA.



LAND PATTERN EXAMPLE
SCALE:4X

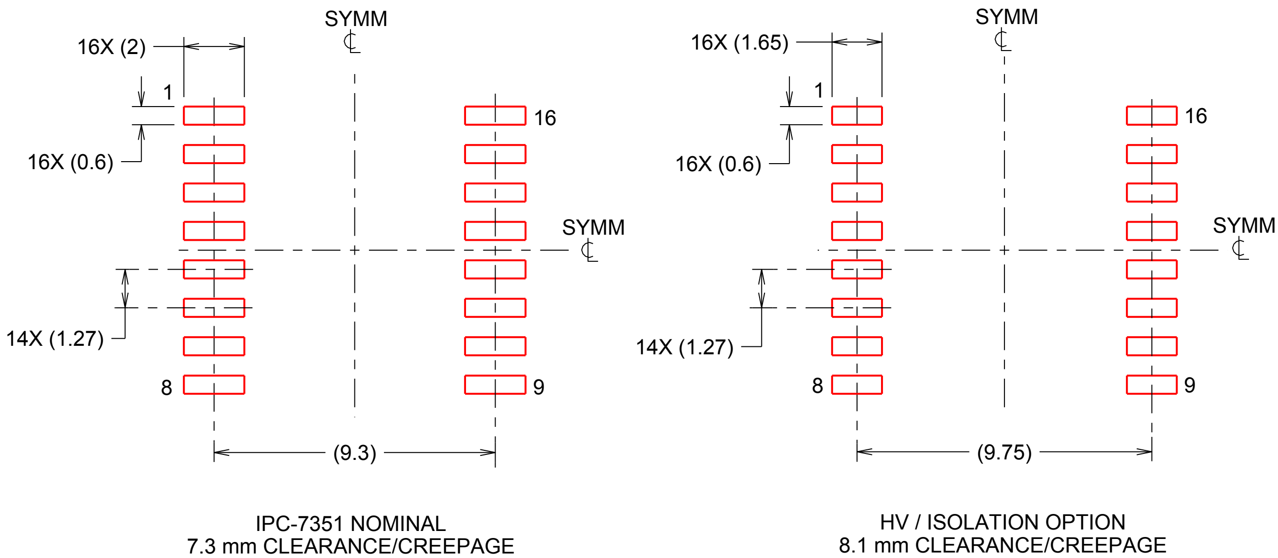


SOLDER MASK DETAILS

4221009/A 08/2013

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/A 08/2013

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO1050DUB	ACTIVE	SOP	DUB	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-55 to 105	ISO1050	Samples
ISO1050DUBR	ACTIVE	SOP	DUB	8	350	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-55 to 105	ISO1050	Samples
ISO1050DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 105	ISO1050	Samples
ISO1050DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 105	ISO1050	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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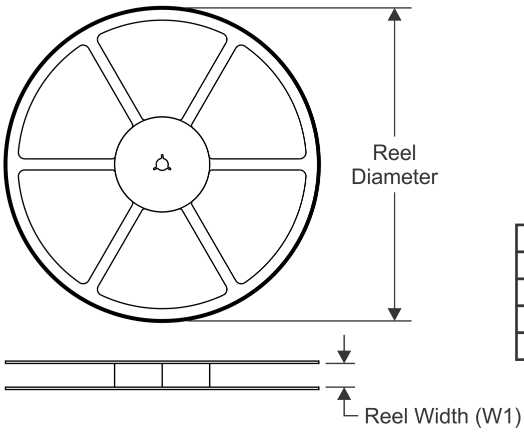
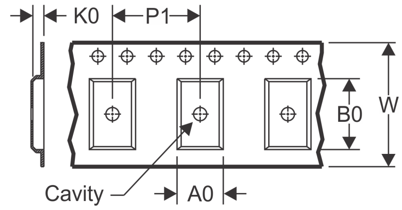
TAPE AND REEL INFORMATION

REEL DIMENSIONS

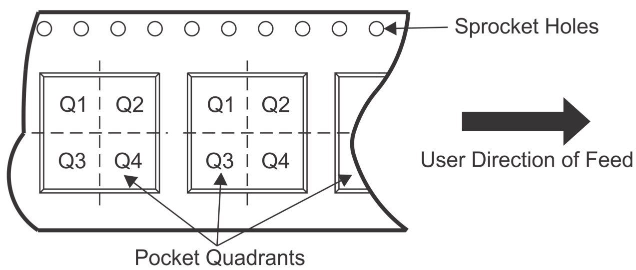


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

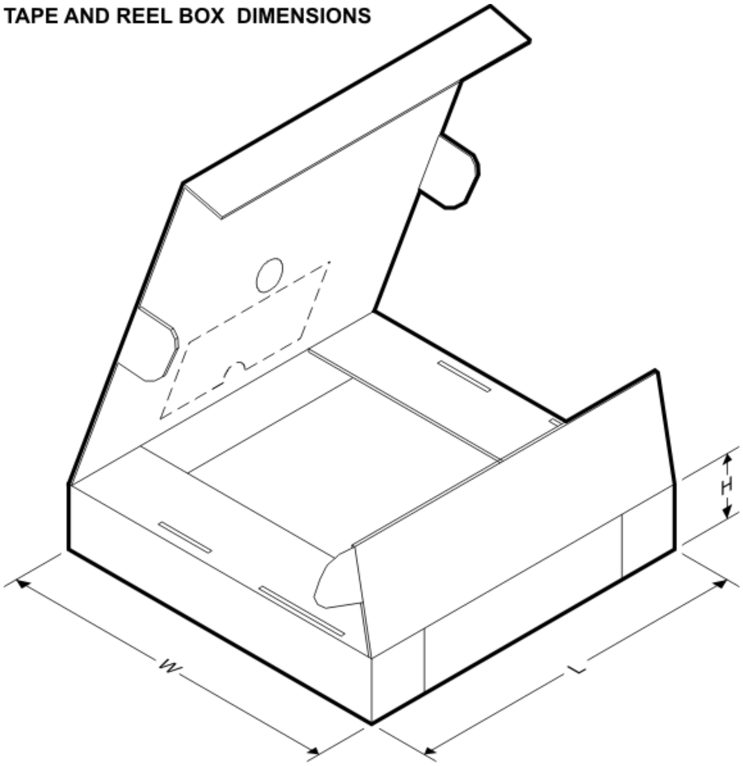
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1050DUBR	SOP	DUB	8	350	330.0	24.4	10.9	10.01	5.85	16.0	24.0	Q1
ISO1050DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

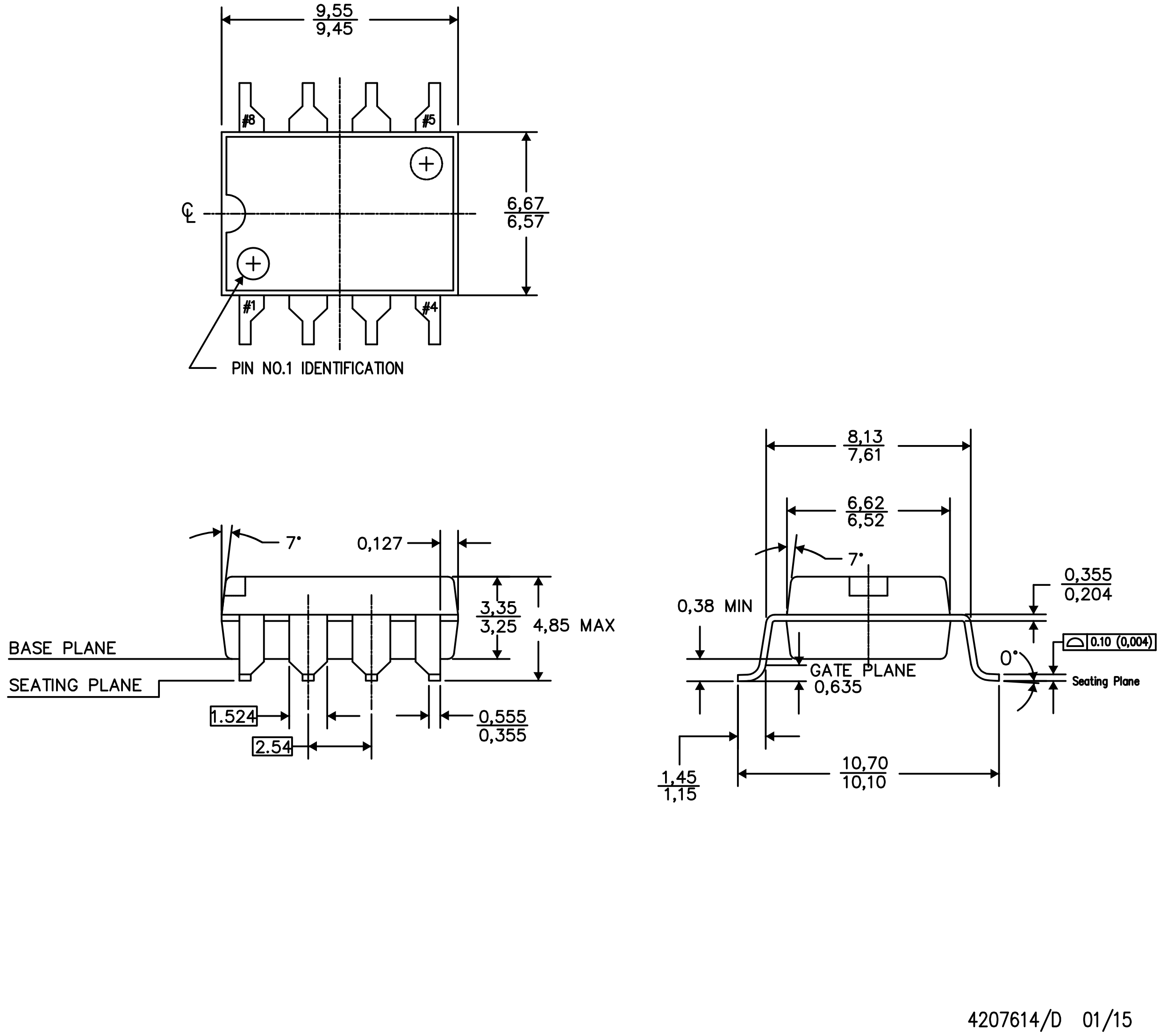
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

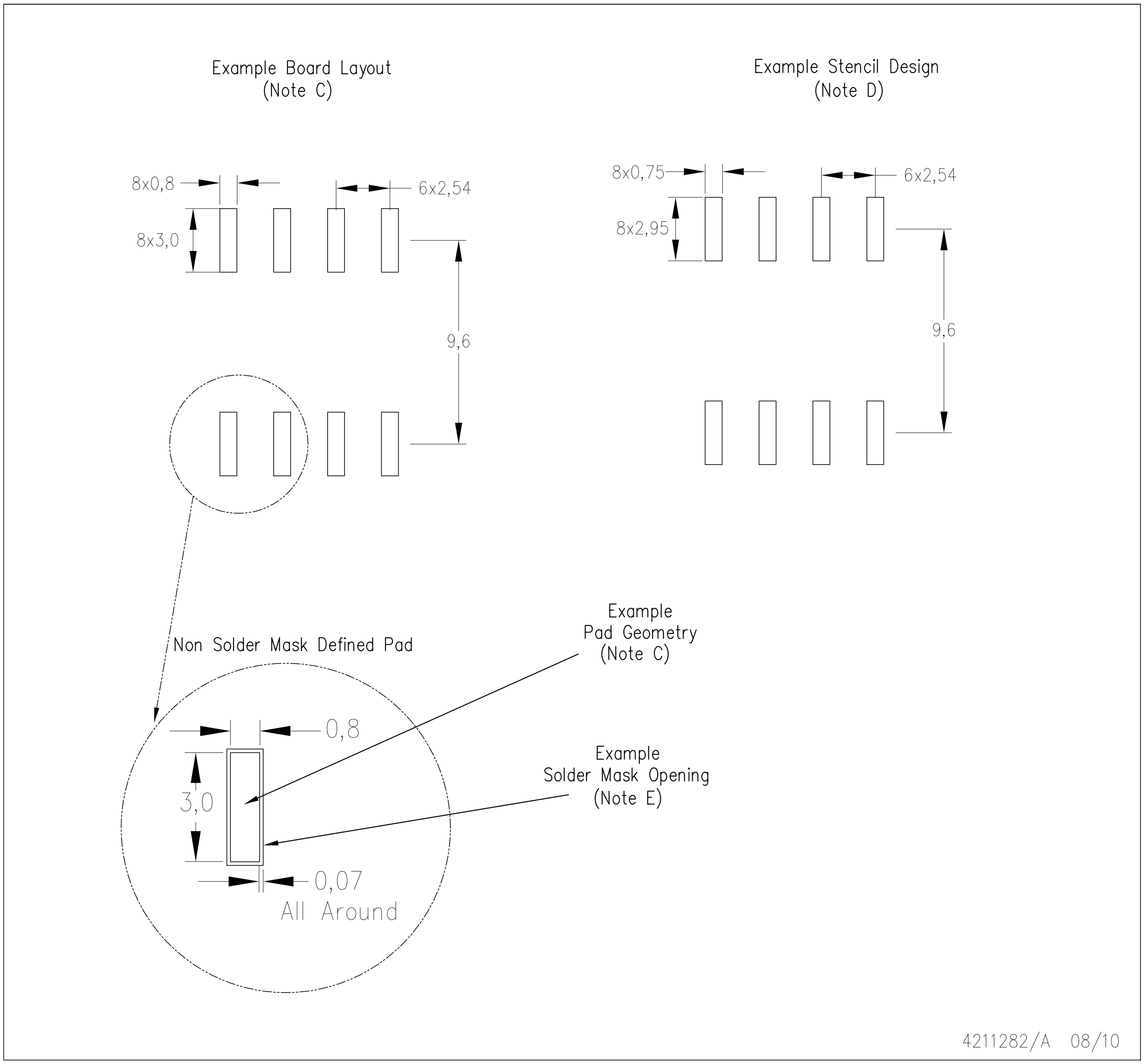
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1050DUBR	SOP	DUB	8	350	406.0	348.0	63.0
ISO1050DWR	SOIC	DW	16	2000	367.0	367.0	38.0

DUB (R-PDSO-G8) PLASTIC SMALL-OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ANSI Y14.5 M-1982.
B. This drawing is subject to change without notice.
C. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.254mm.

DUB (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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