International
IOR Rectifier

August 13th, 2008

# IRS211(7,71,8)(S)

## SINGLE CHANNEL DRIVER

### IC Features

- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20V
- Undervoltage lockout
- CMOS Schmitt-triggered inputs with pull-down
- Output in phase with input
- RoHS compliant
- IRS2117 and IRS2118 also available in PDIP8

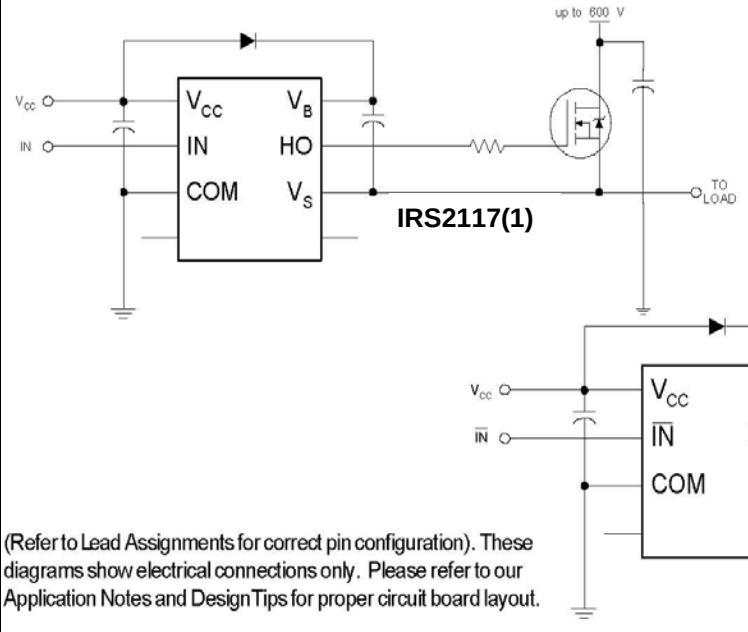
### Product Summary

| | | |
|---|---|---|
| Topology | | Single High Side |
| $V_{OFFSET}$ | | 600 V |
| $V_{OUT}$ | | 10V-20 V |
| $I_{O+}$ & $I_{O-}$ (typical) | | 290 mA & 600 mA |
| IN voltage threshold | IRS211(7,8) | 9.5 V & 6 V |
| | IRS21171 | 2.5 V & 0.8 V |

### Package Type

**SOIC8**

**PDIP8**




(Refer to Lead Assignments for correct pin configuration). These diagrams show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

## Description

The IRS2117, IRS21171, and IRS2118 are high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized mono−lithic construction. The logic input is compatible with standard CMOS outputs. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side or low-side configuration which operates up to 600 V.

## Qualification Information†

| | | | |
|---|---|---|---|
| **Qualification Level** | | Industrial†† (per JEDEC JESD 47) | |
| | | Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level. | |
| **Moisture Sensitivity Level** | | SOIC8 | MSL2††† 260°C (per IPC/JEDEC J-STD-020C) |
| | | PDIP8 | Not applicable (non-surface mount package style) |
| **ESD** | Machine Model | Class B (per JEDEC standard EIA/JESD22-A115) | |
| | Human Body Model | Class 3A (per EIA/JEDEC standard JESD22-A114) | |
| **IC Latch-Up Test** | | Class I, Level A (per JESD78) | |
| **RoHS Compliant** | | Yes | |

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_B$ | High-side floating supply voltage | | -0.3 | 625 | V |
| $V_S$ | High-side floating supply offset voltage | | $V_B$ - 25 | $V_B$ + 0.3 | |
| $V_{HO}$ | High-side floating output voltage | | $V_S$ - 0.3 | $V_B$ + 0.3 | |
| $V_{CC}$ | Logic supply voltage | | - 0.3 | 25 | |
| $V_{IN}$ | Logic input voltage | | - 0.3 | $V_{CC}$ + 0.3 | |
| $dV_S/dt$ | Allowable offset supply voltage transient (fig.2) | | --- | 50 | V/ns |
| $P_D$ | Package power dissipation @ $T_A \leq +25^\circ C$ | 8 lead SOIC | --- | 0.625 | W |
| | | 8 lead PDIP | | 1.0 | |
| $R_{\theta JA}$ | Thermal Resistance, junction to Ambient | 8 lead SOIC | --- | 200 | °C/W |
| | | 8 lead PDIP | | 125 | |
| $T_J$ | Junction temperature | | --- | 150 | °C |
| $T_S$ | Storage temperature | | -55 | 150 | |
| $T_L$ | Lead Temperature (soldering, 10 seconds) | | --- | 300 | |

## Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The VS offset rating is tested with all supplies biased at 15 V differential.

| Symbol | Definition | Min. | Max. | Units |
|---|---|---|---|---|
| $V_B$ | High-Side floating supply absolute voltage | $V_S$ + 10 | $V_S$ + 20 | V |
| $V_S$ | High-side floating supply offset voltage | † | 600 | |
| $V_{HO}$ | High-side floating output voltage | $V_S$ | $V_B$ | |
| $V_{CC}$ | Logic supply voltage | 10 | 20 | |
| $V_{IN}$ | Logic input voltage | 0 | $V_{CC}$ | |
| $T_A$ | Ambient Temperature | -40 | 125 | °C |

† Logic operational for $V_S$ of -5 V to +600 V. Logic state held for $V_S$ of -5 V to – $V_{BS}$.

## Dynamic Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15 V, $C_L$ = 1000 pF and $T_A$ = 25 ° C unless otherwise specified.

| Symbol | Definition | | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{on}$ | Turn-on propagation delay | IRS21171 | --- | 160 | 230 | ns | VS = 0V |
| | | IRS211(7,8) | --- | 125 | 200 | | |
| $t_{off}$ | Turn-off propagation delay | IRS21171 | --- | 160 | 230 | | VS = 600V |
| | | IRS211(7,8) | --- | 105 | 180 | | |
| $t_r$ | Turn-on rise time | | --- | 75 | 130 | | |
| $t_f$ | Turn-off fall time | | --- | 35 | 65 | | |

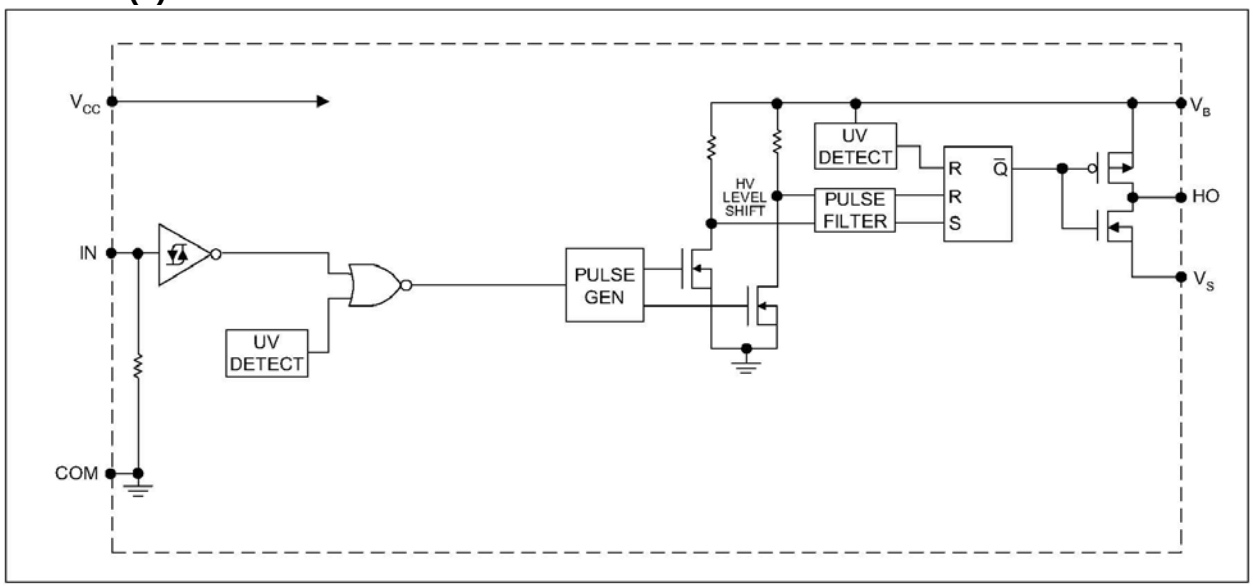
## Static Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15 V and $T_A$ = 25 ° C unless otherwise specified. The $V_{IN}$, $V_{TH}$, and $I_{IN}$ parameters are referenced to COM. The $V_O$ and $I_O$ parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

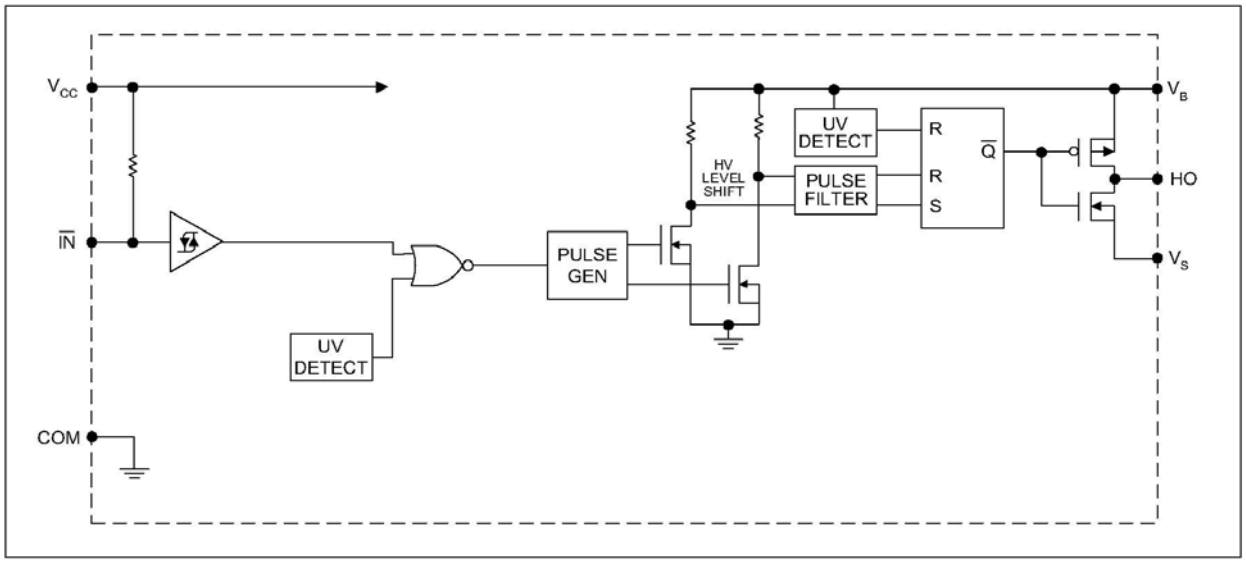
| Symbol | Definition | | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input voltage –logic “1” | IRS21171 | 2.5 | --- | --- | V | |
| | | IRS211(7,8) | 9.5 | --- | --- | | |
| $V_{IL}$ | Input voltage – logic “0” | IRS21171 | --- | --- | 0.8 | | |
| | | IRS211(7,8) | | | 6.0 | | |
| $V_{OH}$ | High level output voltage, $V_{BIAS}$ – $V_O$ | | --- | 0.05 | 0.2 | | $I_O$ = 2mA |
| $V_{OL}$ | Low level output voltage, $V_C$ | | --- | 0.02 | 0.1 | | |
| $I_{LK}$ | Offset supply leakage current | | --- | --- | 50 | µA | $V_B$ = $V_S$ = 600V |
| $I_{QBS}$ | Quiescent $V_{BS}$ Supply Current | IRS211(7,8) | --- | 50 | 240 | | $V_{IN}$ = 0V or $V_{CC}$ |
| | | IRS21171 | --- | 80 | 150 | | |
| $I_{QCC}$ | Quiescent $V_{CC}$ Supply Current | IRS211(7,8) | --- | 70 | 340 | | |
| | | IRS21171 | --- | 120 | 240 | | |
| $I_{IN+}$ | Logic “1” input bias current | IRS2117(1) | --- | 20 | 40 | | $V_{IN}$ = $V_{CC}$ |
| | | IRS2118 | | | | | $V_{IN}$ = 0V |
| $I_{IN-}$ | Logic “0” input bias current | IRS2117(1) | --- | --- | 5.0 | | |
| | | IRS2118 | | | | | $V_{IN}$ = $V_{CC}$ |
| $V_{BSUV+}$ | $V_{BS}$ supply undervoltage positive going | | 7.6 | 8.6 | 9.6 | V | |
| $V_{BSUV-}$ | $V_{BS}$ supply undervoltage negative going | | 7.2 | 8.2 | 9.2 | | |
| $V_{CCUV+}$ | $V_{CC}$ supply undervoltage positive going | | 7.6 | 8.6 | 9.6 | | |
| $V_{CCUV-}$ | $V_{CC}$ supply undervoltage negative going | | 7.2 | 8.2 | 9.2 | | |
| $I_{O+}$ | Output high short circuit pulsed current | | 200 | 290 | --- | mA | $V_O$ = 0V<br>$V_{IN}$ Logic “1”<br>PW ≤ 10 µs |
| $I_{O-}$ | Output low short circuit pulsed current | | 420 | 600 | --- | | $V_O$ = 15V<br>$V_{IN}$ Logic “0”<br>PW ≤ 10 µs |

## Functional Block Diagram

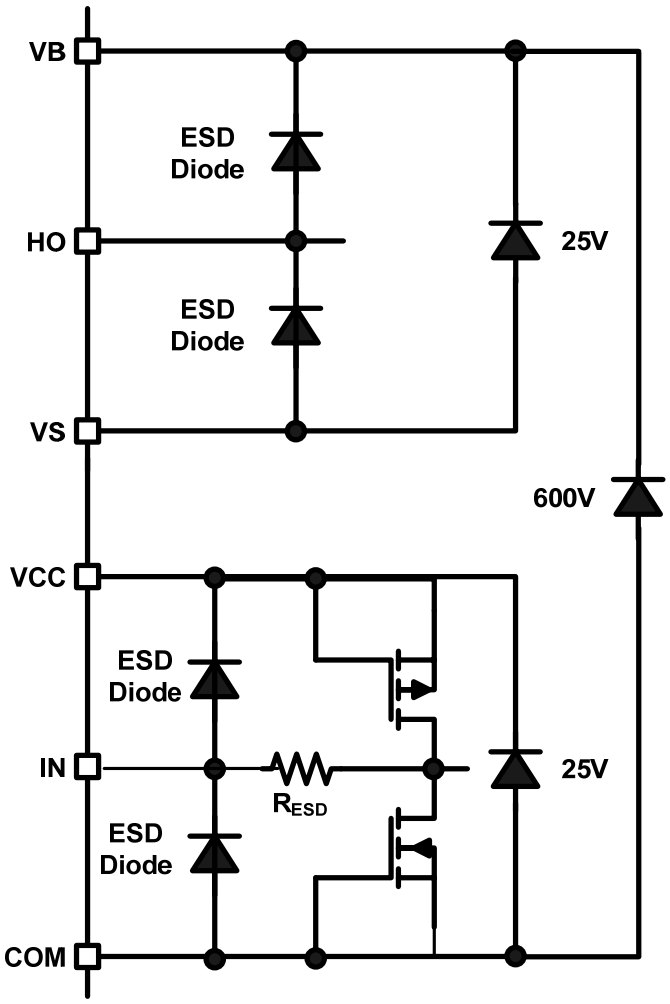
### IRS2117(1)




### IRS2118



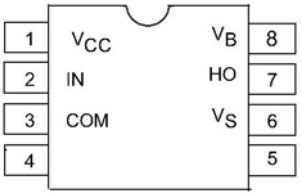
**I/O Pin Equivalent Circuit Diagrams: IRS211(7,71,8)**



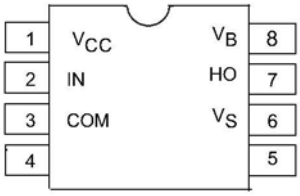
## Lead Definitions

| Pin # | Symbol | Description |
|---|---|---|
| 1 | VCC | Logic and gate drive supply |
| 2 | IN | IRS2117(1) Logic input for gate driver output (HO), in phase with HO |
| | /IN | IRS2118 Logic input for gate driver output (HO), in phase with HO |
| 3 | COM | Logic ground |
| 4 | NC | No Connect |
| 5 | NC | No Connect |
| 6 | $V_B$ | High-side floating supply |
| 7 | HO | High-side gate drive output |
| 8 | $V_S$ | High-side floating supply return |

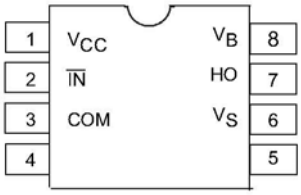
## Lead Assignments



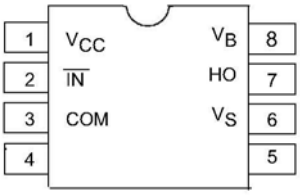

**PDIP 8**
**IRS2117(1)**




**SOIC 8**
**IRS2117(1)**




**PDIP 8**
**IRS2118**




**SOIC 8**
**IRS2118**

## Application Information and Additional Details

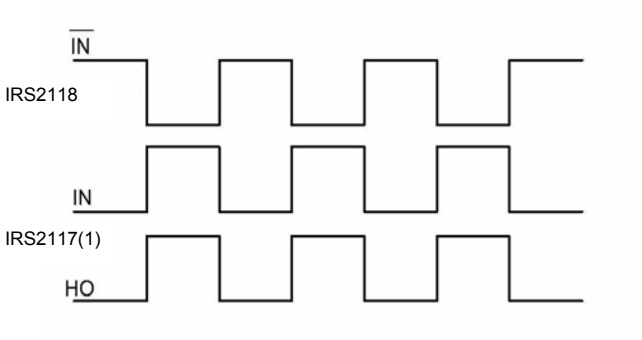



**Figure 1 Input/Output Timing Diagram circuit**

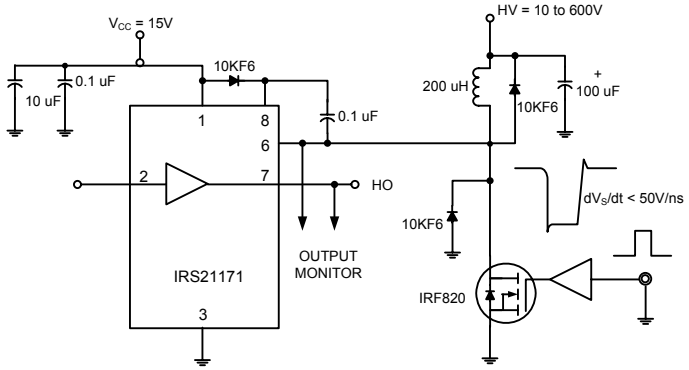



**Figure 2 Floating Supply Voltage Transient Test circuit**

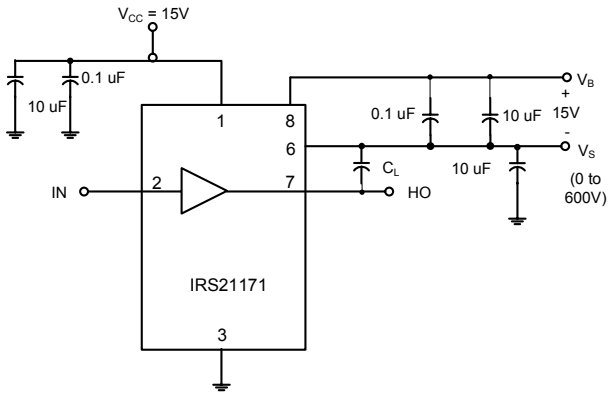



**Figure 3 Switching Time Test Circuit**

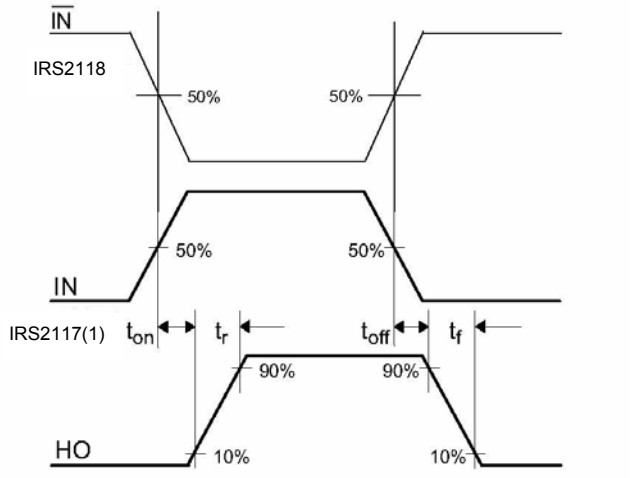



**Figure 4 Switching Time Waveform Definition**

## Parameter Temperature Trends - 211(7,71,8)

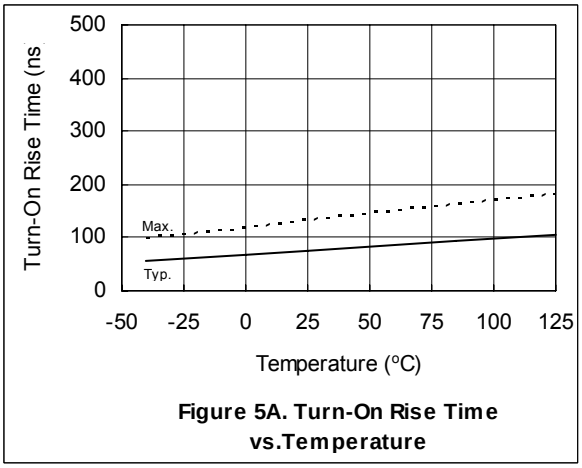



**Figure 5A. Turn-On Rise Time vs.Temperature**

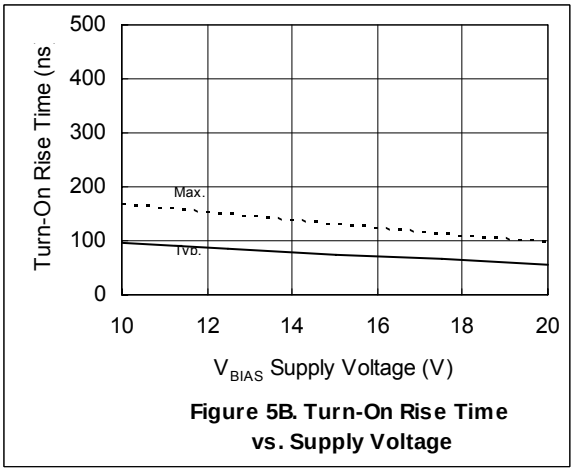



**Figure 5B. Turn-On Rise Time vs. Supply Voltage**

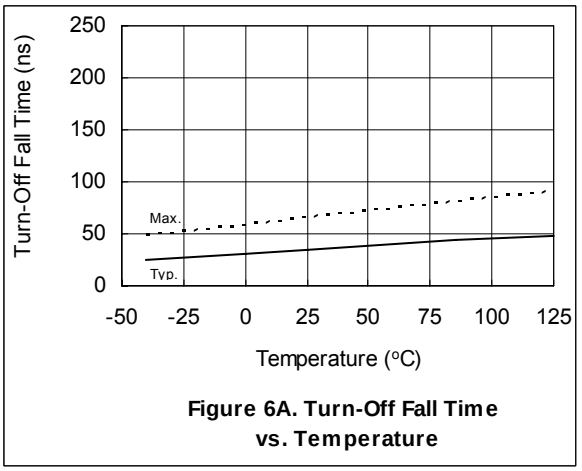



**Figure 6A. Turn-Off Fall Time vs. Temperature**

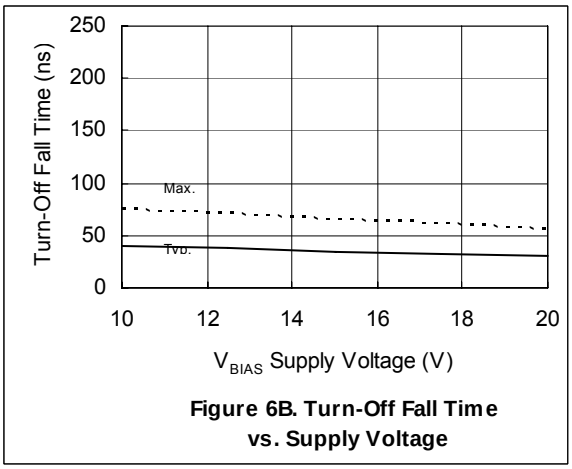



**Figure 6B. Turn-Off Fall Time vs. Supply Voltage**

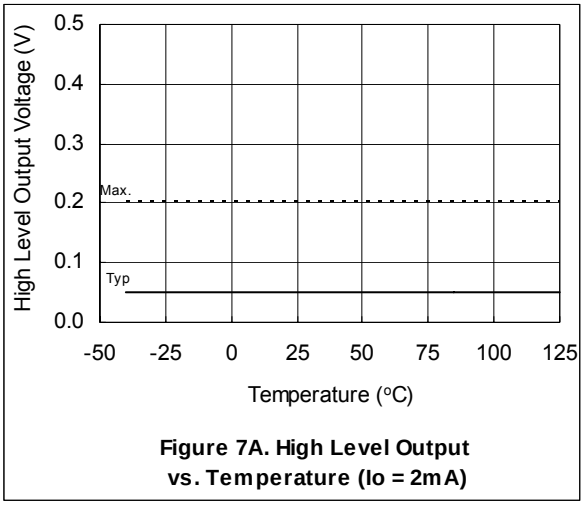



**Figure 7A. High Level Output vs. Temperature (Io = 2mA)**

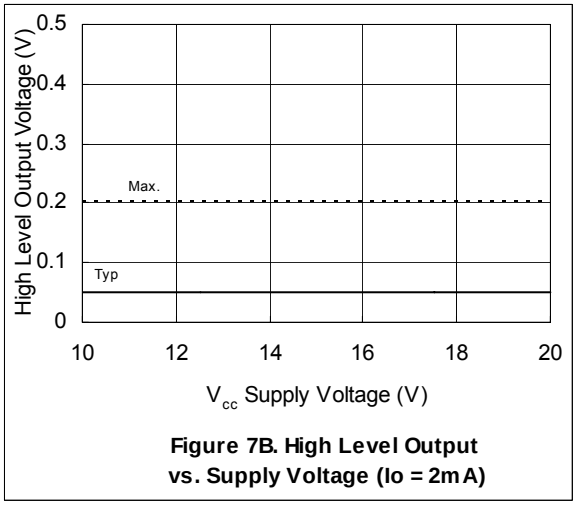



**Figure 7B. High Level Output vs. Supply Voltage (Io = 2mA)**

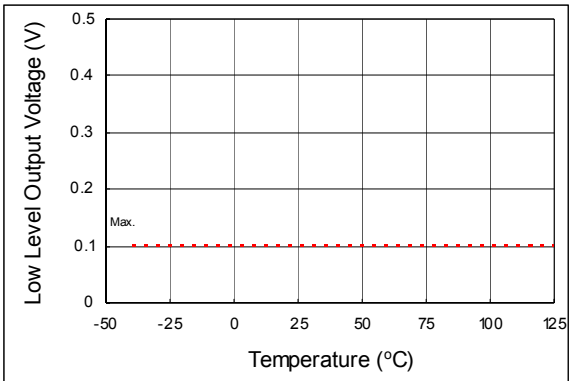



**Figure 8A. Low Level Output vs.Temperature**

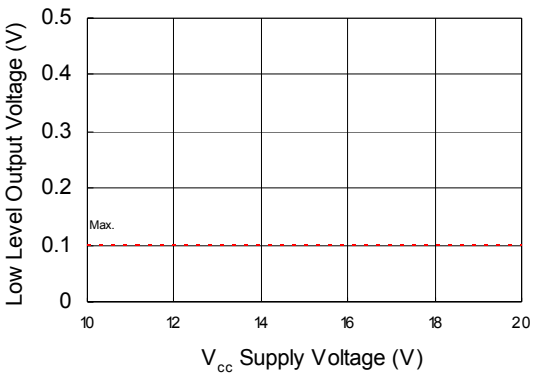



**Figure 8B. Low Level Output vs. Supply Voltage**

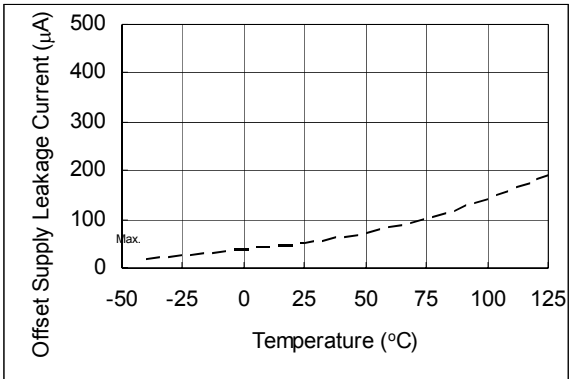



**Figure 9A. Offset Supply Leakage Current vs. Temperature**

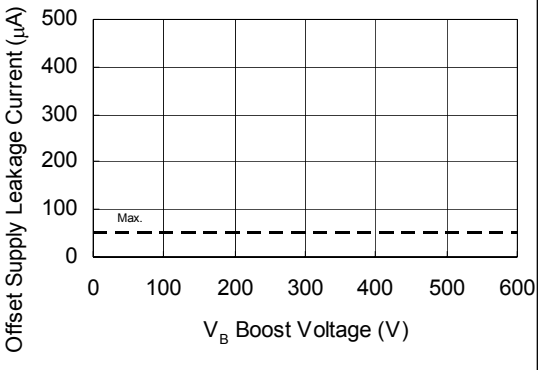



**Figure 9B.Offset Supply Leakage Current vs. VB Boost Voltage**

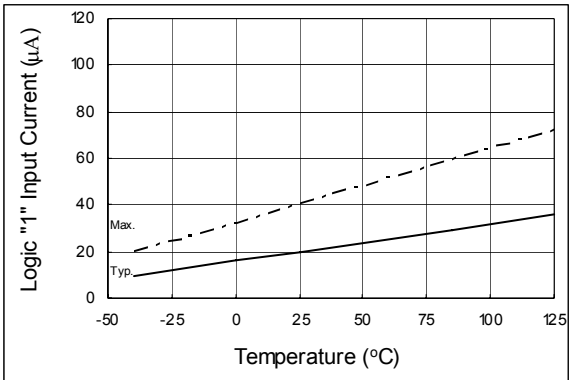



**Figure 10A. Logic "1" (2118 "0") Input Current vs. Temperature**

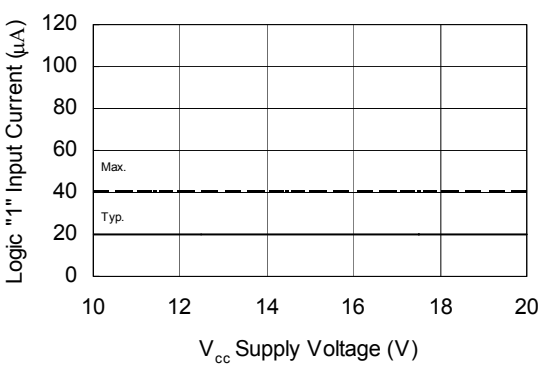



**Figure 10B. Logic "1" (2118 "0") Input Current vs. Supply Voltage**

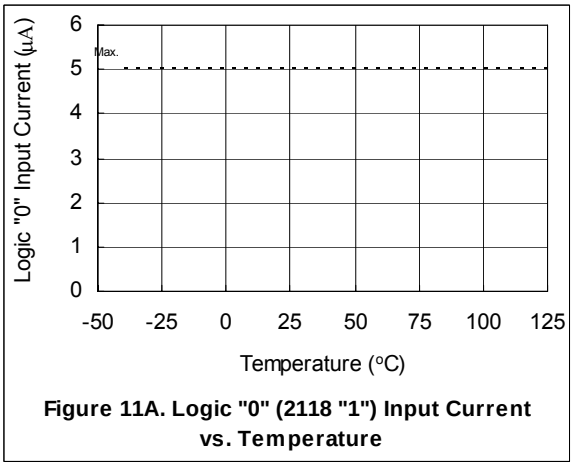



**Figure 11A. Logic "0" (2118 "1") Input Current vs. Temperature**

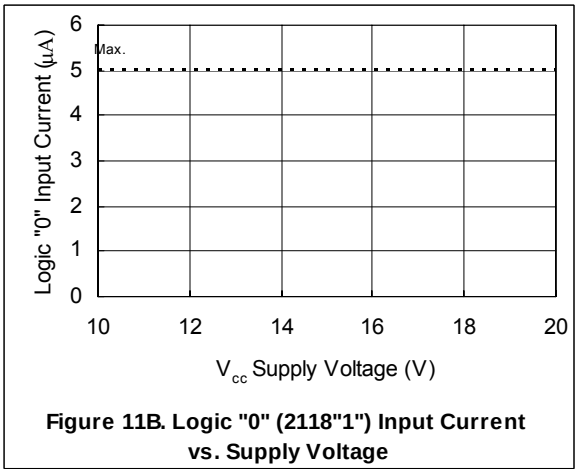



**Figure 11B. Logic "0" (2118"1") Input Current vs. Supply Voltage**

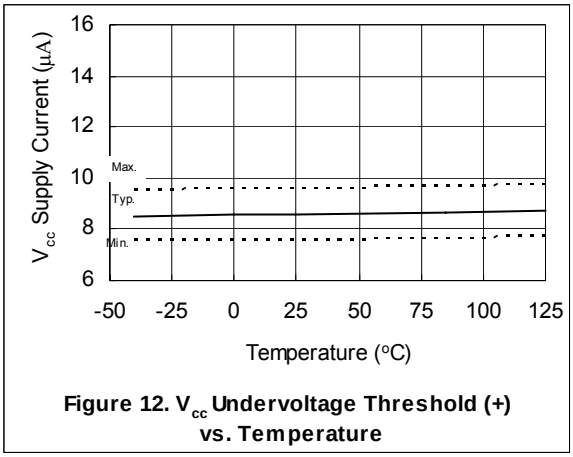



**Figure 12. $V_{cc}$ Undervoltage Threshold (+) vs. Temperature**

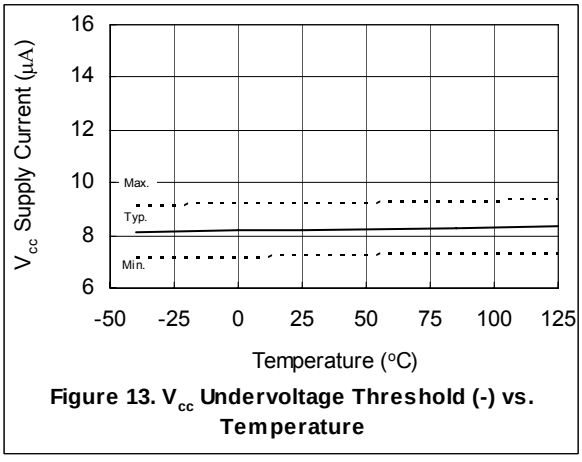



**Figure 13. $V_{cc}$ Undervoltage Threshold (-) vs. Temperature**

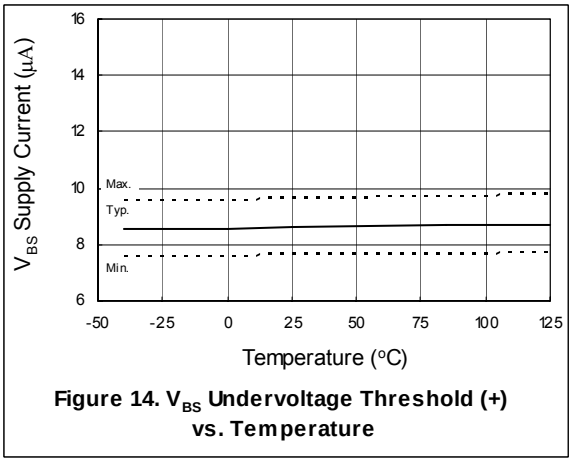



**Figure 14. $V_{BS}$ Undervoltage Threshold (+) vs. Temperature**

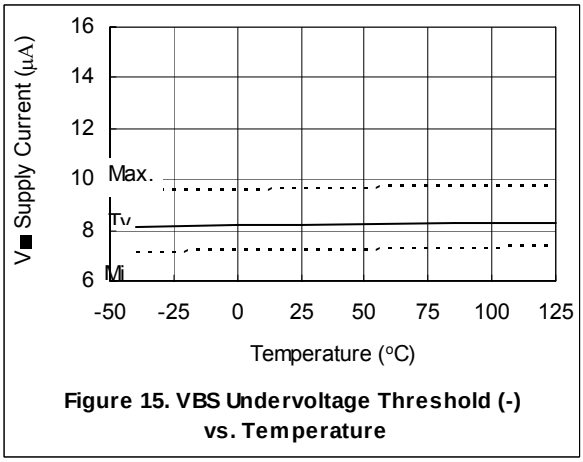



**Figure 15. VBS Undervoltage Threshold (-) vs. Temperature**

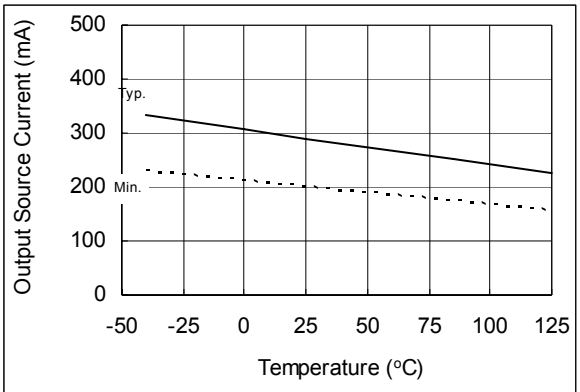



**Figure 16A. Output Source Current vs. Temperature**

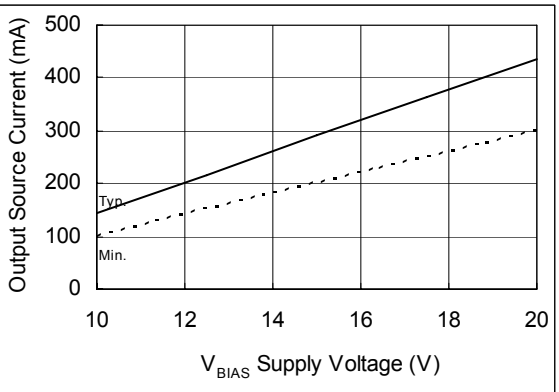



**Figure 16B. Output Source Current vs. Supply Voltage**

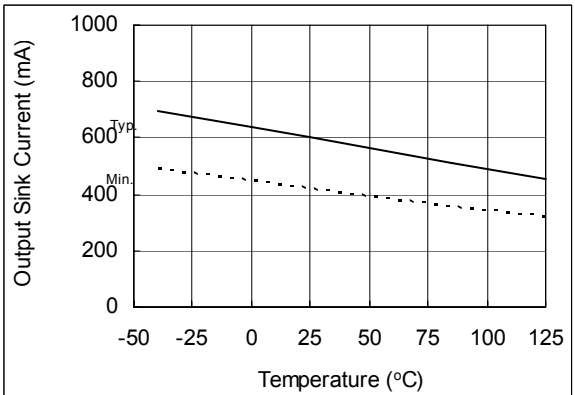



**Figure 17A. Output Sink Current vs.Temperature**

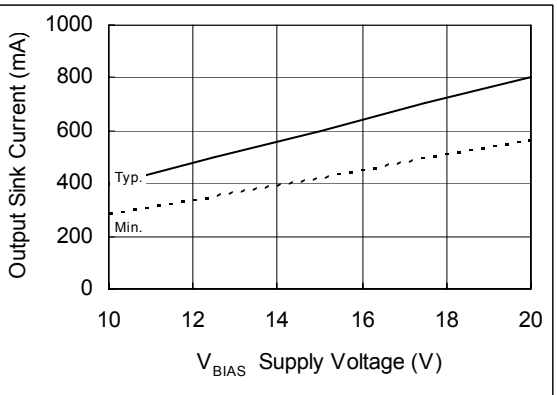



**Figure 17B. Output Sink Current vs. Supply Voltage**

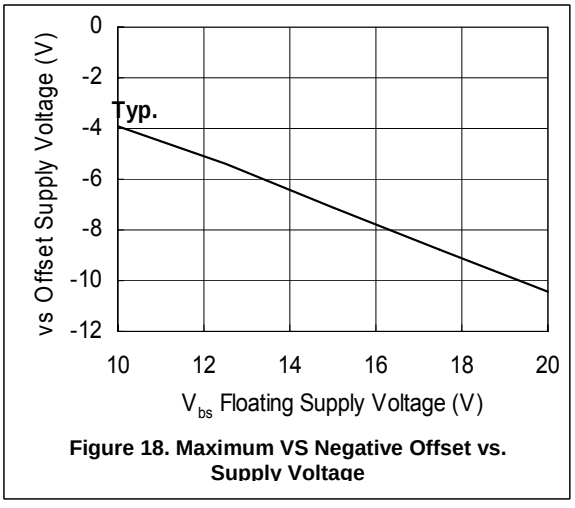



**Figure 18. Maximum VS Negative Offset vs. Supply Voltage**

## Parameter Temperature Trends - 211(7,8)

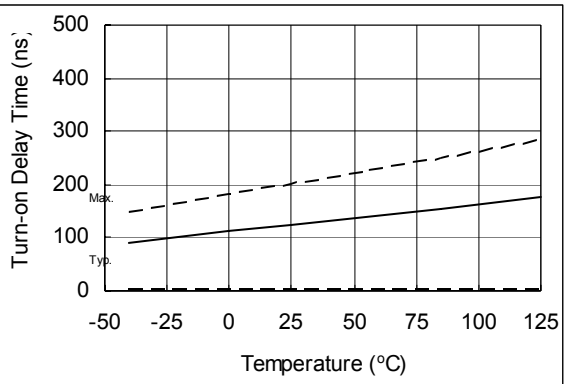



**Figure 19A. IRS211(7,8) Turn-On Time vs. Temperature**

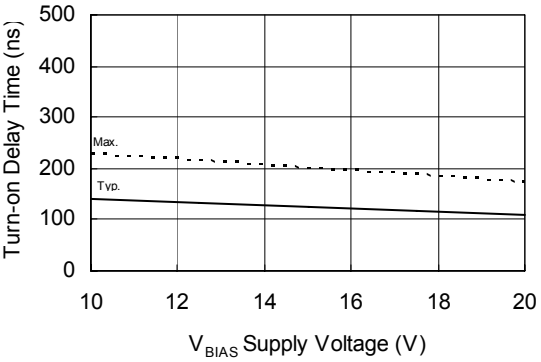



**Figure 19B. IRS211(7,8) Turn-On Time vs. Supply Voltage**

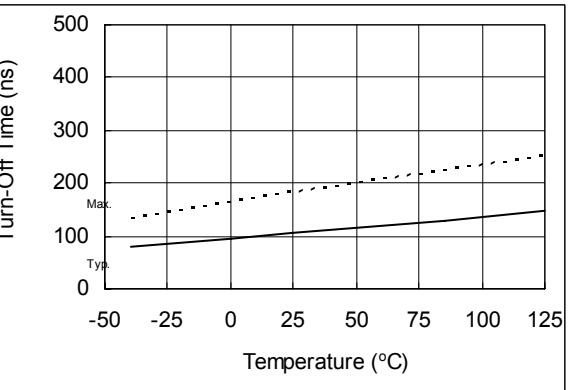



**Figure 20A. IRS211(7,8) Turn-Off Time vs. Temperature**

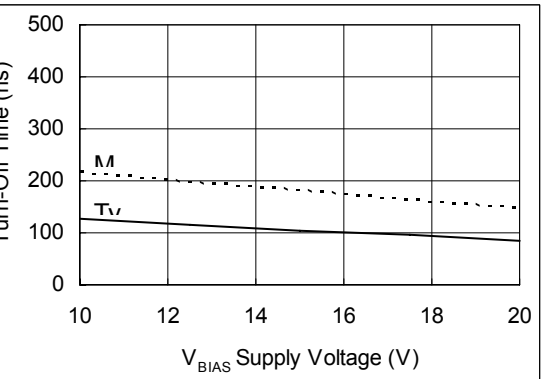



**Figure 20B. IRS211(7,8) Turn-Off Time vs. Supply Voltage**

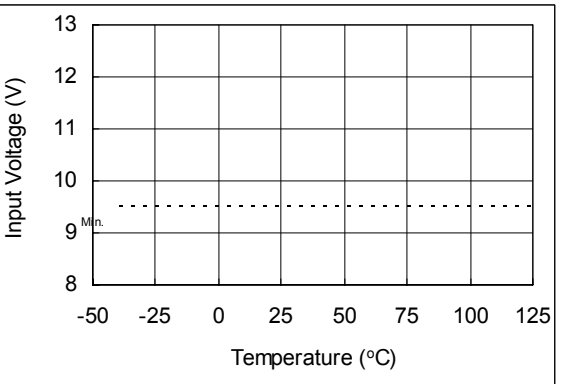



**Figure 21A. IRS2117 Logic "1" (2118 "0") Input Voltage vs. Temperature**

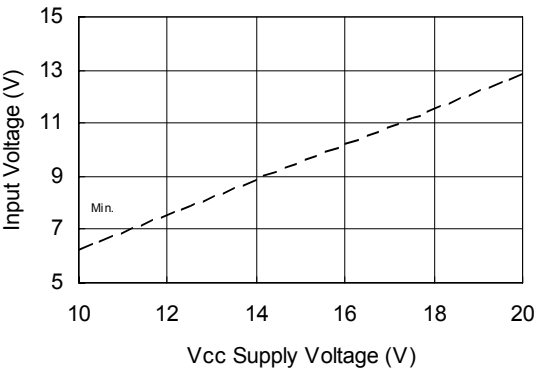



**Figure 21B. IRS2117 Logic "1" (2118 "0") Input Voltage vs. Supply Voltage**

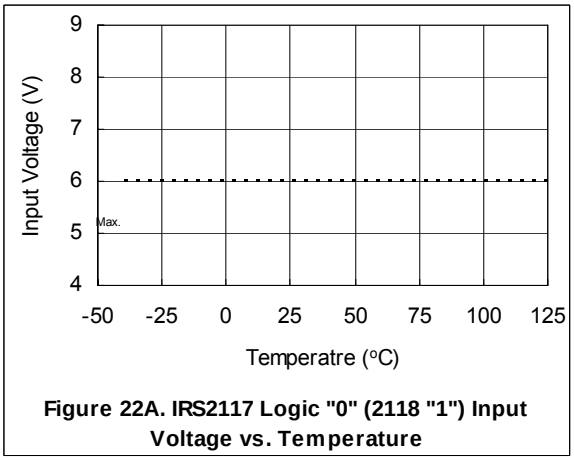



**Figure 22A. IRS2117 Logic "0" (2118 "1") Input Voltage vs. Temperature**

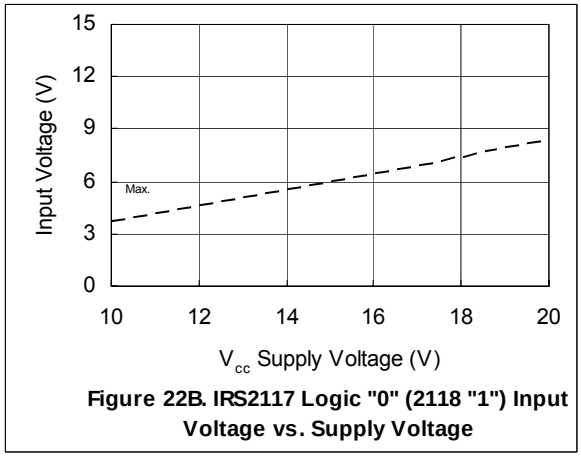



**Figure 22B. IRS2117 Logic "0" (2118 "1") Input Voltage vs. Supply Voltage**

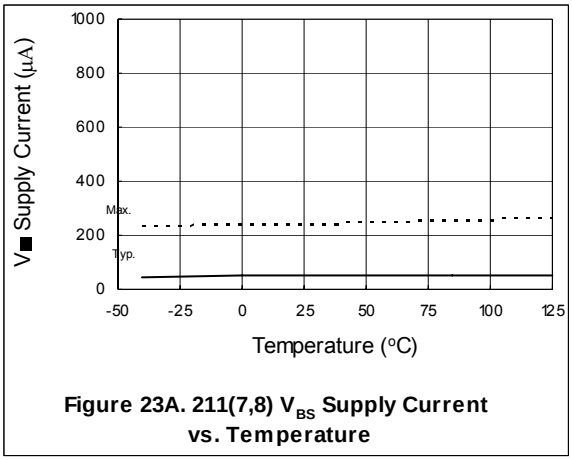



**Figure 23A. 211(7,8) $V_{BS}$ Supply Current vs. Temperature**

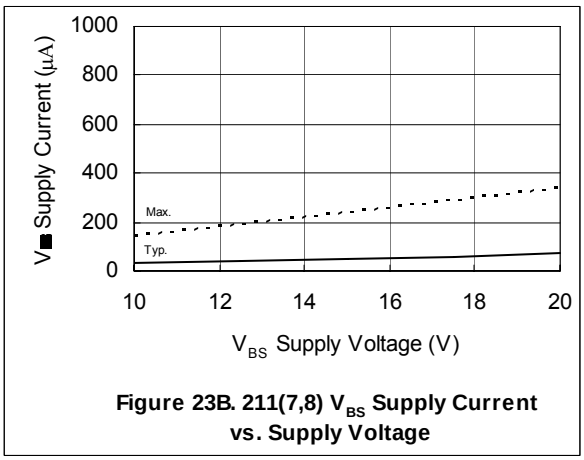



**Figure 23B. 211(7,8) $V_{BS}$ Supply Current vs. Supply Voltage**

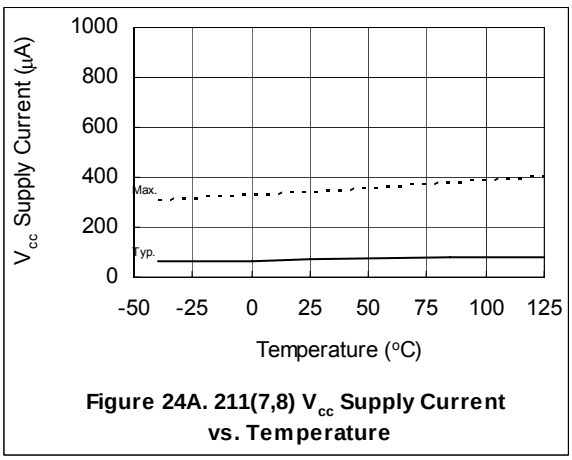



**Figure 24A. 211(7,8) $V_{cc}$ Supply Current vs. Temperature**

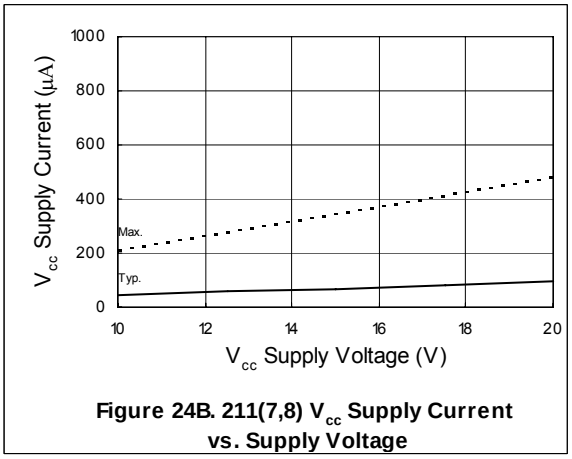



**Figure 24B. 211(7,8) $V_{cc}$ Supply Current vs. Supply Voltage**

## Parameter Temperature Trends - 21171

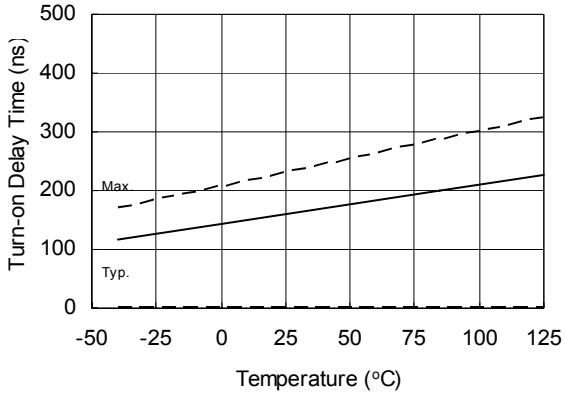



**Figure 25A. IRS21171 Turn-On Time vs. Temperature**

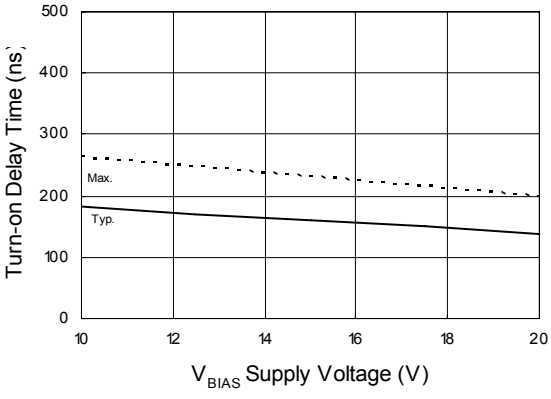



**Figure 25B. IRS21171 Turn-On Time vs. Supply Voltage**

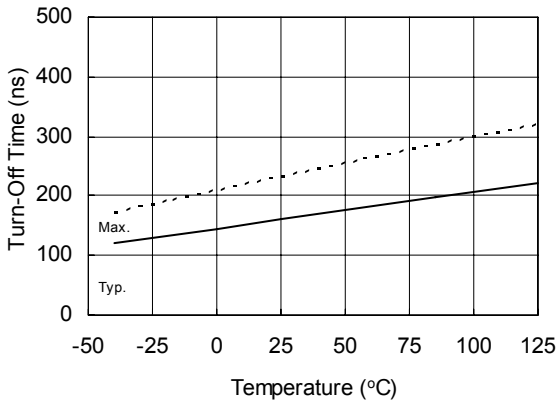



**Figure 26A. IRS21171 Turn-Off Time vs. Temperature**

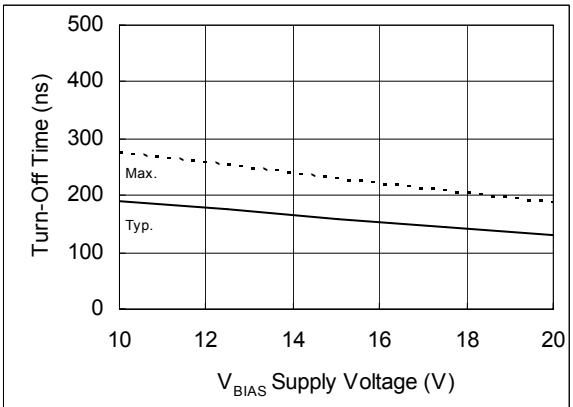



**Figure 26B. IRS21171 Turn-Off Time vs. Supply Voltage**

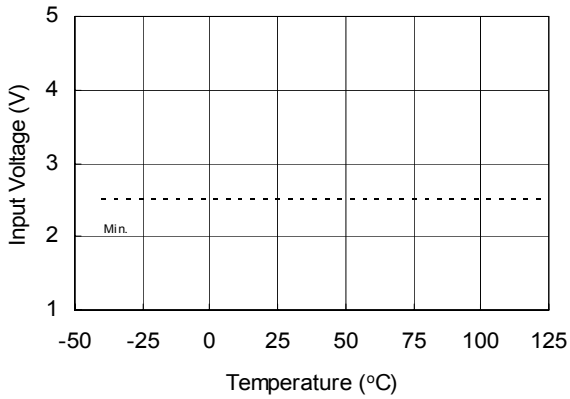



**Figure 27A. IRS21171 Logic "1" Input Voltage vs. Temperature**

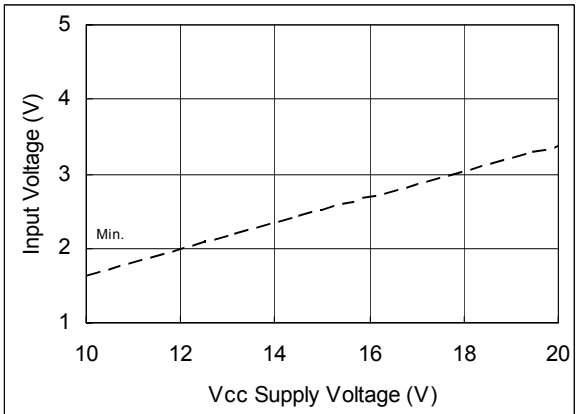



**Figure 27B. IRS21171 Logic "1" Input Voltage vs. Supply Voltage**

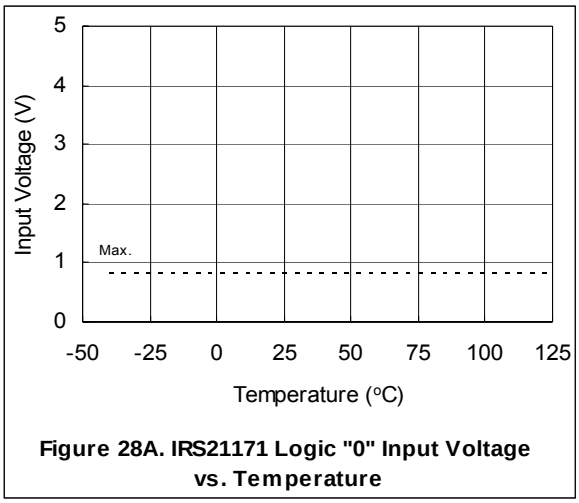



**Figure 28A. IRS21171 Logic "0" Input Voltage vs. Temperature**

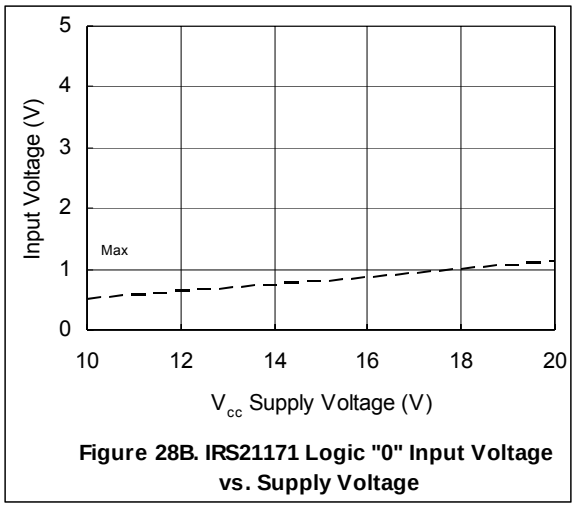



**Figure 28B. IRS21171 Logic "0" Input Voltage vs. Supply Voltage**

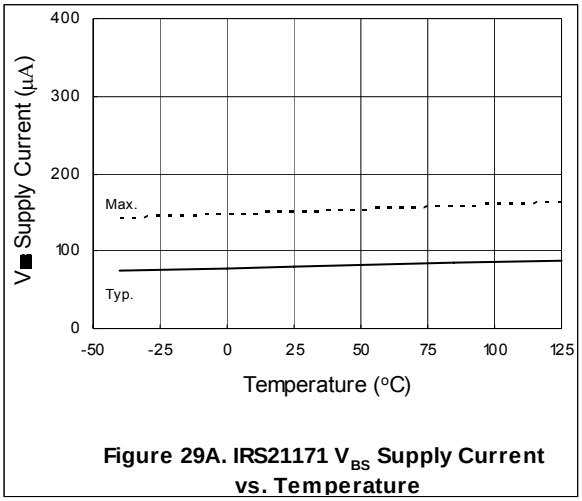



**Figure 29A. IRS21171 $V_{BS}$ Supply Current vs. Temperature**

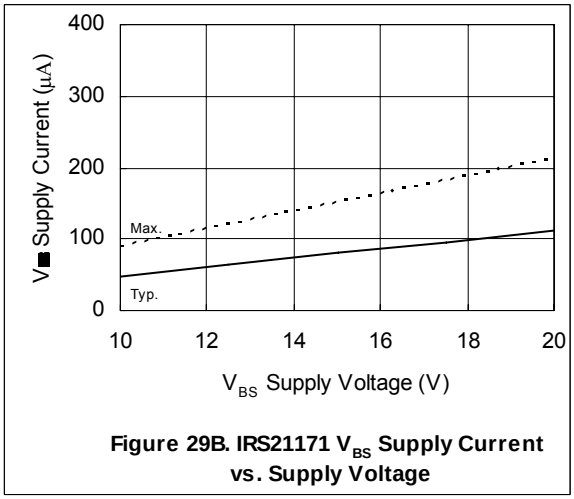



**Figure 29B. IRS21171 $V_{BS}$ Supply Current vs. Supply Voltage**

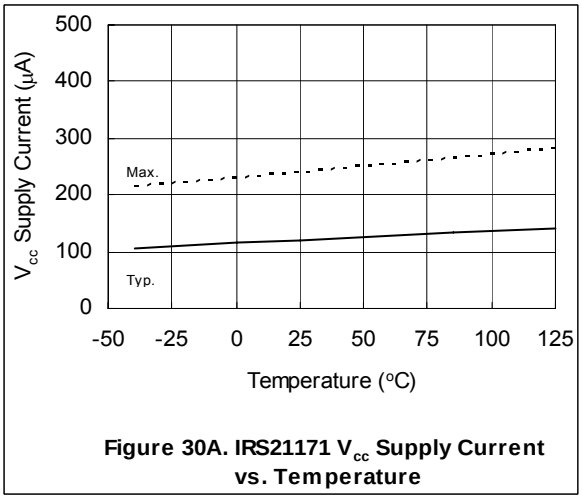



**Figure 30A. IRS21171 $V_{cc}$ Supply Current vs. Temperature**

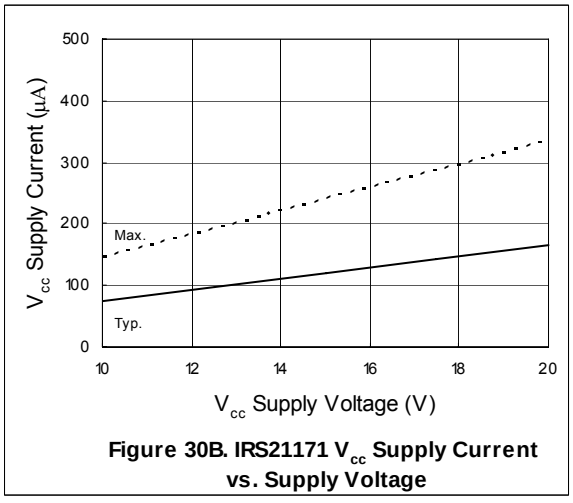



**Figure 30B. IRS21171 $V_{cc}$ Supply Current vs. Supply Voltage**

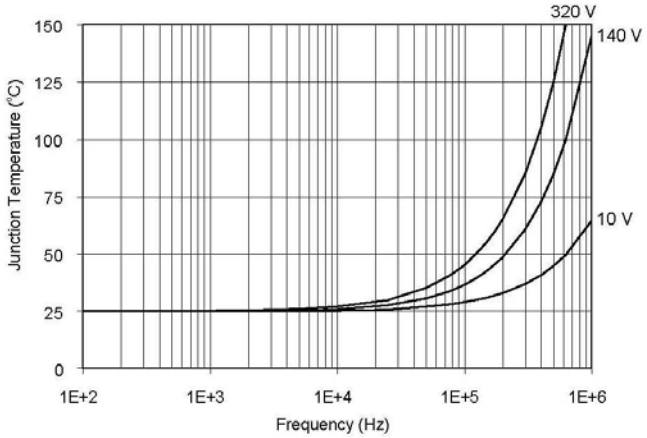



**Figure 24. IRS2117/IRS2118 $T_J$ vs. Frequency (IRFBC20)**
**$R_{GATE}$ = 33 Ω, $V_{CC}$ = 15 V**

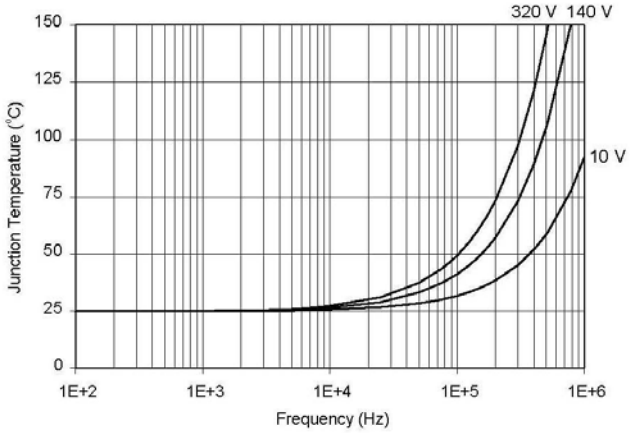



**Figure 25. IRS2117/IRS2118 $T_J$ vs. Frequency (IRFBC30)**
**$R_{GATE}$ = 22 Ω, $V_{CC}$ = 15 V**

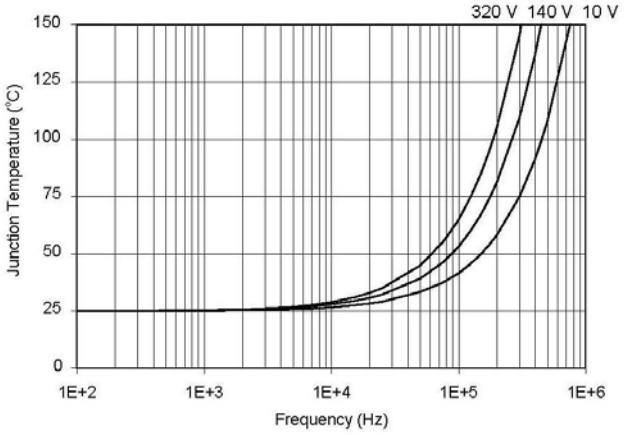



**Figure 26. IRS2117/IRS2118 $T_J$ vs. Frequency (IRFBC40)**
**$R_{GATE}$ = 15 Ω, $V_{CC}$ = 15 V**

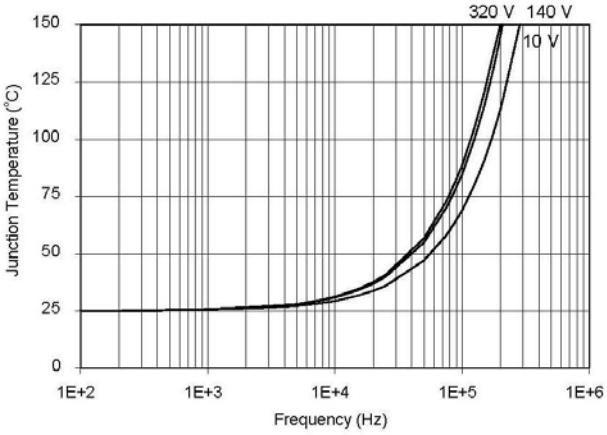
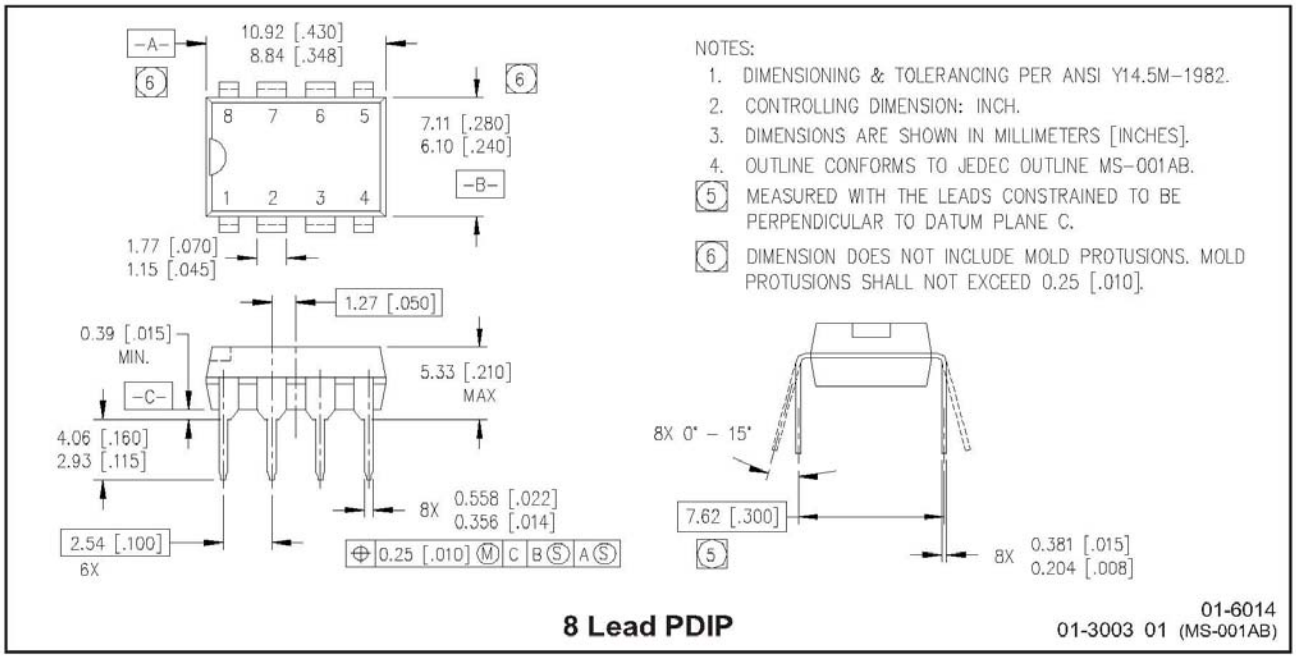


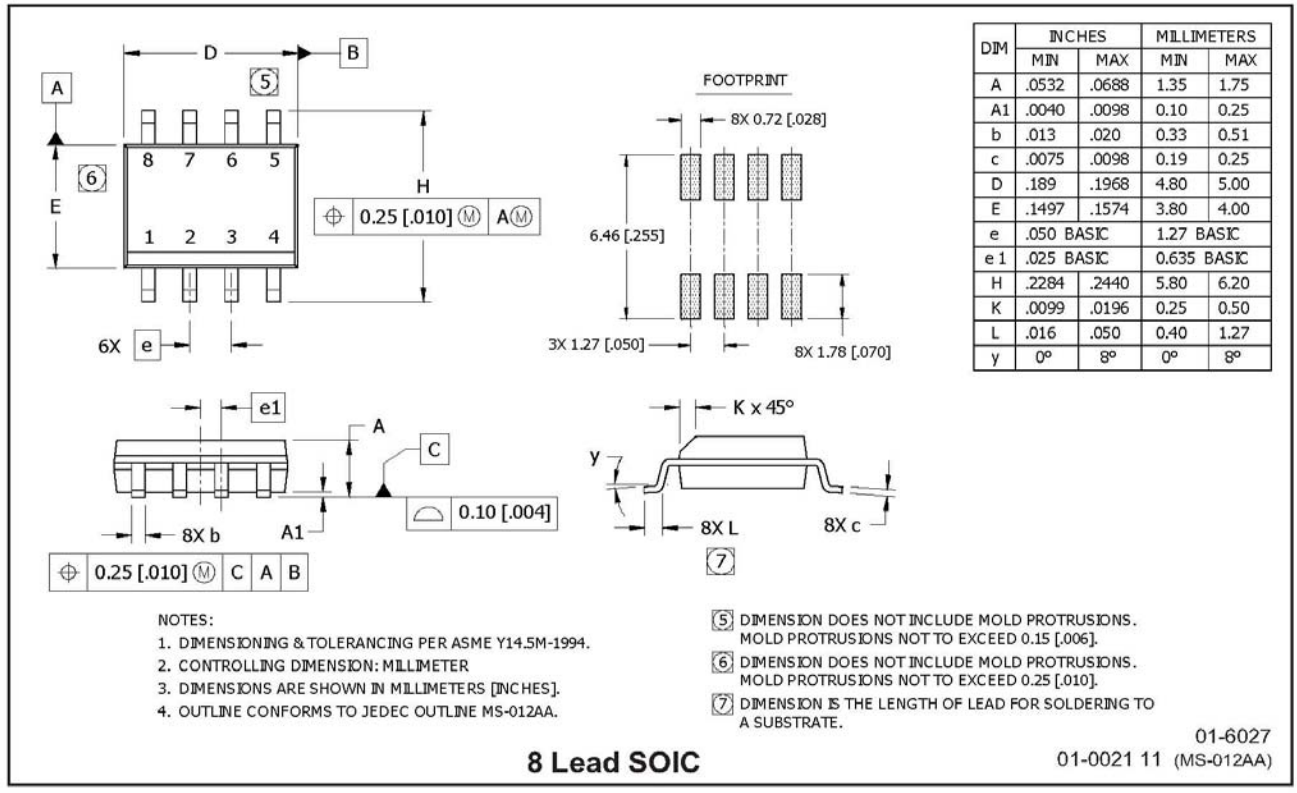

**Figure 27. IRS2117/IRS2118 $T_J$ vs. Frequency (IRFPE50)**
**$R_{GATE}$ = 10 Ω, $V_{CC}$ = 15 V**

## Package Details




**8 Lead PDIP**

01-6014
01-3003 01 (MS-001AB)

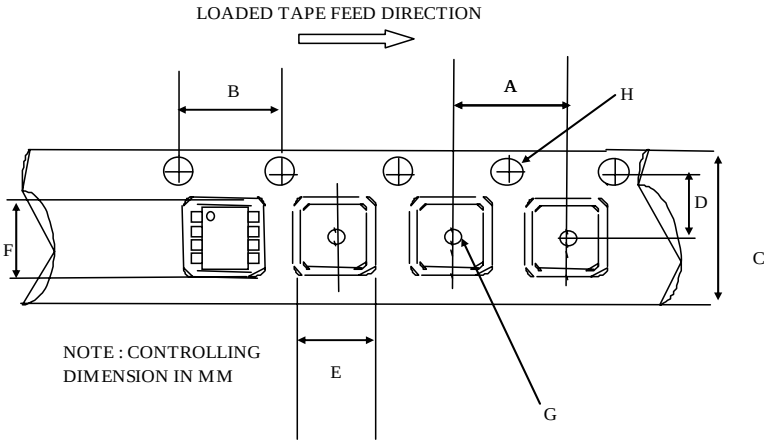



| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .0532 | .0688 | 1.35 | 1.75 |
| A1 | .0040 | .0098 | 0.10 | 0.25 |
| b | .013 | .020 | 0.33 | 0.51 |
| c | .0075 | .0098 | 0.19 | 0.25 |
| D | .189 | .1968 | 4.80 | 5.00 |
| E | .1497 | .1574 | 3.80 | 4.00 |
| e | .050 BASIC | | 1.27 BASIC | |
| e 1 | .025 BASIC | | 0.635 BASIC | |
| H | .2284 | .2440 | 5.80 | 6.20 |
| K | .0099 | .0196 | 0.25 | 0.50 |
| L | .016 | .050 | 0.40 | 1.27 |
| y | 0° | 8° | 0° | 8° |

**8 Lead SOIC**

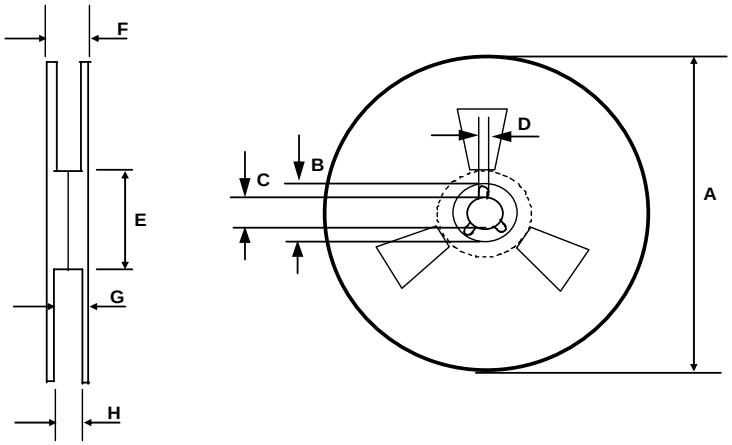
01-6027
01-0021 11 (MS-012AA)

## Package Details: SOIC8N, Tape and Reel




CARRIER TAPE DIMENSION FOR 8SOICN

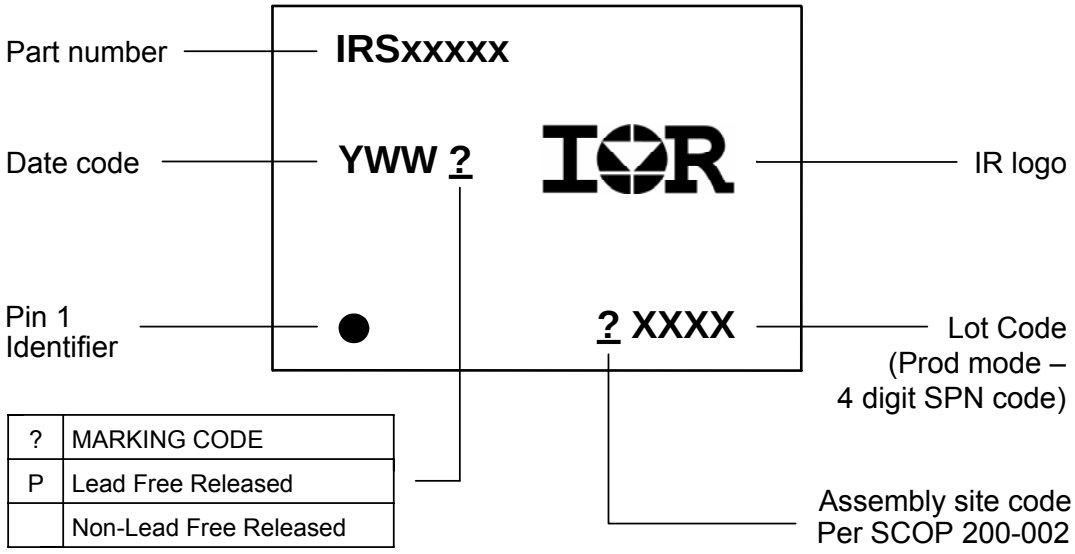
| | Metric | | Imperial | |
|---|---|---|---|---|
| Code | Min | Max | Min | Max |
| A | 7.90 | 8.10 | 0.311 | 0.318 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 11.70 | 12.30 | 0.46 | 0.484 |
| D | 5.45 | 5.55 | 0.214 | 0.218 |
| E | 6.30 | 6.50 | 0.248 | 0.255 |
| F | 5.10 | 5.30 | 0.200 | 0.208 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |




REEL DIMENSIONS FOR 8SOICN

| | Metric | | Imperial | |
|---|---|---|---|---|
| Code | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 18.40 | n/a | 0.724 |
| G | 14.50 | 17.10 | 0.570 | 0.673 |
| H | 12.40 | 14.40 | 0.488 | 0.566 |

**Part Marking Information**




| | |
|---|---|
| ? | MARKING CODE |
| P | Lead Free Released |
| | Non-Lead Free Released |

## Ordering Information

| Base Part Number | Package Type | Standard Pack | | Complete Part Number |
|---|---|---|---|---|
| | | Form | Quantity | |
| IRS2117 | SOIC8N | Tube/Bulk | 95 | IRS2117SPBF |
| | | Tape and Reel | 2500 | IRS2117STRPBF |
| | PDIP8 | Tube/Bulk | 50 | IRS2117PBF |
| IRS21171 | SOIC8N | Tube/Bulk | 95 | IRS21171SPBF |
| | | Tape and Reel | 2500 | IRS21171STRPBF |
| IRS2118 | SOIC8N | Tube/Bulk | 95 | IRS2118SPBF |
| | | Tape and Reel | 2500 | IRS2118STRPBF |
| | PDIP8 | Tube/Bulk | 50 | IRS2118PBF |



For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

WORLD HEADQUARTERS:
233 Kansas St., El Segundo, California 90245
Tel: (310) 252-7105

Revision History

History:

| Date | Change |
|---|---|
| November 11th, 2006 | • IRS211(7,8)(S) data sheet posted on www.irf.com |
| August 13th, 2008 | • IRS21171S is released for data sheet posting on www.irf.com. Data sheet is merged with IRS211(7,8)(S) one, and posted on www.irf.com<br>• Added “IN Voltage threshold in the product summary table |

Qualification Rating: Industrial MSL2, Lead Free

International
IOR Rectifier

http://www.irf.com